



ECDR-814x USER MANUAL

Revision 3.0

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About This Manual

This manual provides information to simplify your installation, configuration, and operation of the ECDR-814x board.

About This Manual describes the contents of each chapter, lists applicable documents, and provides document conventions and technical support information.

Chapters Overview

About This Manual – Describes each chapter in this users manual and provides technical support information.

Chapter 1 Introduction – Provides a general overview of the ECDR-814x, lists the product models available, and describes operating modes and product applications

Chapter 2 Product Overview – Provides additional product information including analog signal inputs, clocking, channel configurations, and analog-to-digital data.

Chapter 3 Specifications – Provides general and environmental specifications, and power requirements for the ECDR-814x board.

Chapter 4 Installation and Setup – Provides board installation and setup information, including setting switches and connectors.

Chapter 5 Operating Guide – Provides information for connecting inputs to signal sources, configuring the VME Bus and the AD6620s, and synchronizing operation and control. This chapter also includes examples of data collection modes.

Chapter 6 Register Maps – Provides memory maps and registers for the ECDR-814x board.

Applicable Documents

The following sources provide important reference information for installing and configuring the ECDR-814x board.

- CY7C960 and CY7C961 User's guide, Cypress Semiconductor Corp.
- AD6644 Data Specification, Analog Devices Corp.
- AD6620 Data Specification, Analog Devices Corp.
- [RACE++ Product Specification, Echotek Corp.](#)
- ANSI/VITA 1-1994 (VME64 Specification)
- ANSI/VITA 1.1-1997 (VME64 Extensions Specification)
- ANSI/VITA 5.1-1999 (RACEway Interlink Specification)
- The VMEBus Handbook, VMEbus International Trade Association (VITA)
- [ECDR-814x Programmers Manual, Echotek Corp.](#)
- RACE++ Series: RACEway Interlink Modules Data Sheet, Mercury Computer Systems Inc.
- RACE++ Series: Dual-Port RACEway Interlink Modules Data Sheet, Mercury Computer Systems Inc.

Document Conventions

The following icons are used in this manual to emphasize setup or system information.

Icon	Use
	Alerts you to important details regarding the setup or maintenance of your system.
	Alerts you to potential damage to the board during system setup and installation.

Technical Support

If you need additional technical information or assistance in retrieving product documentation, contact Echotek Corporation.

Telephone: 256.721.1911
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Chapter 1 Introduction

This chapter provides a general overview of the ECDR-814x, lists the product models available, and describes operating modes and product applications.

ECDR-814x

Echotek Corporation's ECDR-814x is an analog-to-digital (A/D) converter and digital drop receiver board. The ECDR-814x provides eight receiver channels of 14-bit, 65 MHz analog-to-digital conversion and digital processing suitable for wideband and narrowband down conversion and filtering in a single 6U VME slot. The data for each receiver channel can be programmed for decimation by a factor of 2 to 16384. Refer to Figure 1-1 for the ECDR-814x block diagram.

For applications requiring raw A/D data *only*, the ECDR-814x A/D is available. However, since the receiver section of each channel can be bypassed to output raw A/D, the standard ECDR-814x board (without the digital receiver chips) can also be used for applications requiring raw A/D data. All configuration options are available in two-, four-, or eight-channel models.

Features

- Analog Devices AD6644 converter
- Analog Devices AD6620 digital receiver chip
- Eight channels, 14-bit, 65 MHz analog-to-digital conversion
- User-programmable data decimation from 2 to 16384
- Configuration options available in two, four, or eight channel models
- SFDR in excess of 90 dBFS (decibels full scale)
- FIFO buffer is 16K x 32 bits; factory configurable up to 128K x 32 bits
- VME64X and RACE++ interfaces
- Gain and No Gain models available
- Two operating modes: Gate Mode and Counted Burst
- User-configurable inputs: fixed full-scale of 1.1 Vpp (+5 dBm) or programmable gain input from 12dBm to 19dBm in 1 dB steps

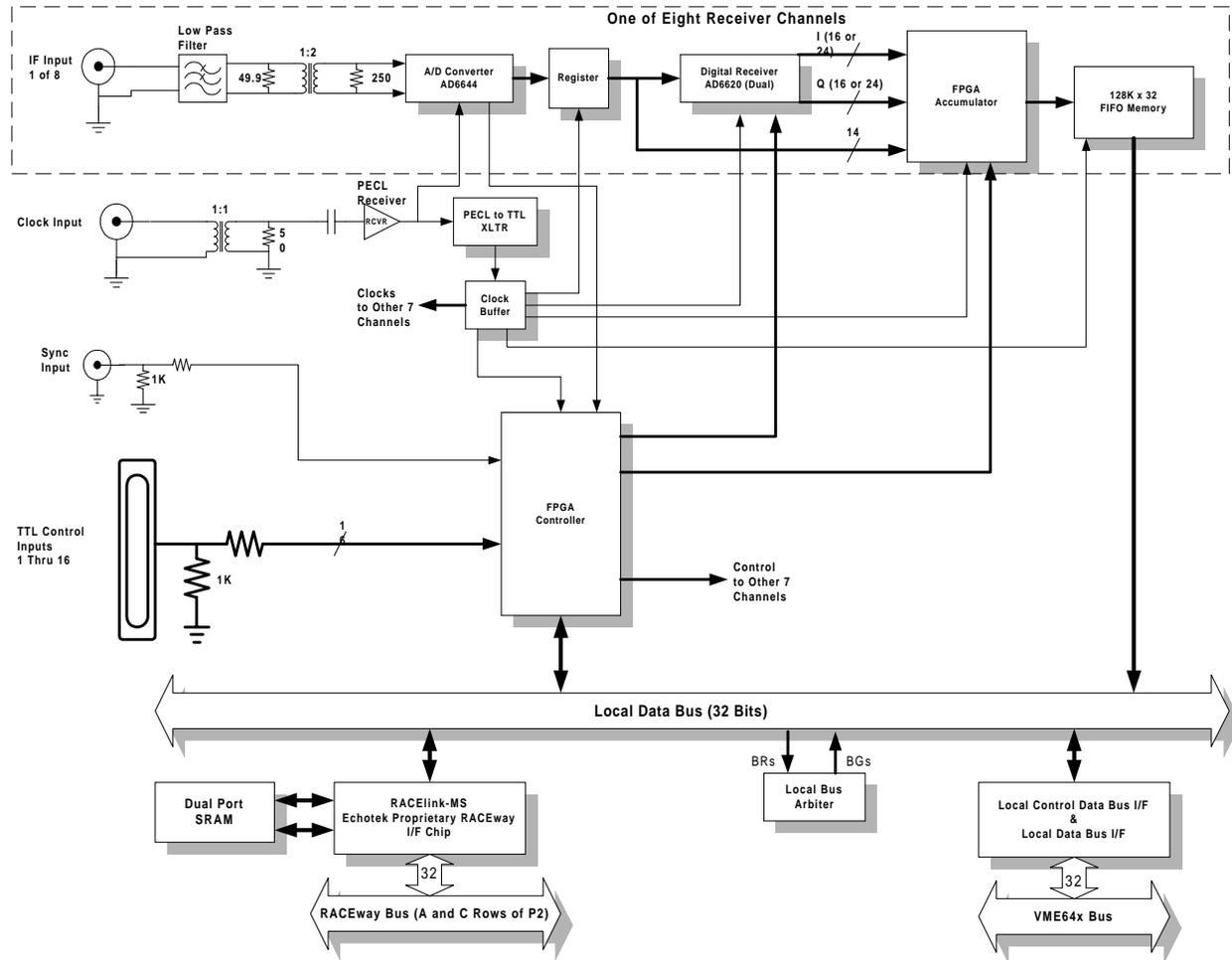


Figure 1-1 ECDR-814x Block Diagram

ECDR-814x Models

The following list includes the ECDR-814x models that are currently available from Echotek Corporation. See Chapter 2 Product Overview for additional information. For additional configurations, please contact [Echotek Corporation](#).

Table 1-1 ECDR-814x – No Gain

Model	Features
ECDR-814/8	Eight channels with two receiver chips per channel
ECDR-814/4	Four channels with two receiver chips per channel
ECDR-814/2	Two channels with two receiver chips per channel
ECDR-814/8-A/D	Eight A/D channels, no receiver chips
ECDR-814/4-A/D	Four A/D channels, no receiver chips
ECDR-814/2-A/D	Two A/D channels, no receiver chips

Table 1-2 ECDR-814x – Gain

Model	Features
ECDR-814G/8	Eight channels with two receiver chips per channel with attenuation and gain
ECDR-814G/4	Four channels with two receiver chips per channel with attenuation and gain
ECDR-814G/2	Two channels with two receiver chips per channel with attenuation and gain
ECDR-814G/8-A/D	Eight A/D channels, no receiver chips with attenuation and gain
ECDR-814G/4-A/D	Four A/D channels, no receiver chips with attenuation and gain
ECDR-814G/2-AD	Two AD channels, no receiver chips with attenuation and gain

Data Inputs

The ECDR-814x board is designed to receive the following inputs through the front panel SMA connectors:

- Eight analog signals
- A/D clock
- Sync signal
- Up to a 16-bit wide digital word

The eight analog signals that can be input to the ECDR-814x board through the front panel SMA connectors are converted using Analog Devices AD6644, 14-bit, 65 MHz A/D converters. The A/D converters are of high quality and exhibit spur free dynamic ranges (SFDR) in excess of 90 dBFS. In addition, the converters support direct digitization for Intermediate Frequencies (IF) up to 100 MHz.

The A/D clock, sync signal, and up to a 16-bit digital word also can be input through the front panel SMA connector. The clock signal (sinewave into 50 ohms) is buffered and distributed to all eight channels so that all channels are sampled simultaneously. The 16-bit wide digital word is normally used to insert a header into the data stream or for tagging data.

Receiver

The Analog Devices AD6620 digital receiver chip provides the digital down converter and filtering, and consists of four signal-processing elements: a digital tuner, two fixed coefficient decimating filters, and a programmable coefficient decimating filter. Each of the eight channels employs dual AD6620s to permit decimation in the Finite Impulse Response (FIR) section by one-half the number of taps (coefficients).

Sample Accumulator

The sample accumulator is a field programmable gate array (FPGA) that outputs the sum of a programmed number of samples from the receiver channels, or if in receiver bypass mode, from the A/D converter. The output can be the sum of 1, 2, 4, 8, 16, 32, 64, 128, or 256 raw A/D samples or In-Phase (I)s, or Quadrature (Q)s (with receiver included).

FIFO Buffer

The FIFO buffer for each channel receives data that is output from the sample accumulator. The FIFO buffer is 16K x 32 bits (by default) and can be configured at the factory as large as 128K x 32 bits.

Data Output

Depending on the model selected, the data output from the ECDR-814/x can be raw A/D data, complex receiver data, and either of the quadrature components. The data can be output through the RACE++ interface and the VME64X interface. Designed for control in real time, the VME64X interface is not optimized for high-speed data transfer.

Operating Modes

The ECDR-814x supports both continuous waveform (CW) and pulsed system applications. The board can be controlled in either of two basic operating modes:

Gate Mode - Data acquisition occurs when the gate signal is active. The gate signal can be provided through external front panel input or by a *write* software function.

Counted Burst - A preprogrammed number of samples is acquired and processed with each occurrence of an external trigger pulse. This trigger pulse also has a software bit counterpart associated with it.

Set-Up and Control

You can access all set-up and control registers through the VME interface. The RACE++ interface can be programmed by either VME or RACE++ and can be a RACE++ master or slave. Refer to Chapter 4 Installation and Setup for more information.

Board Maintenance

The ECDR-814x's "Programmable Logic," in the form of Electrically Programmable Logic Devices (EPLDs) and FPGAs, provides the flexibility to make design modifications required for specific applications. The EPLDs and FPGAs are re-programmable on the board, enabling you to add new "features" as the need arises or to make "bug" fixes.

Note: For upgrading and retesting, please return the ECDR-814/x to the vendor.

ECDR-814/x Applications

The ECDR-814x is a "generic" multi-channel receiver and is designed for applications such as radar, both pulsed and CW, Magnetic Resonance Imaging (MRI) (pulsed), and CW. The following subsections provide additional information on these applications. See Chapter 2 Product Overview for related information on clocking and channel configuration.

- Typical Pulsed
- Typical Continuous Waveform
- Narrow Pulse

Typical Pulsed Application Usage

In general, pulsed applications involve a Pulse Repetition Frequency (PRF) to determine the rate that data collection sequences must occur. A “trigger” pulse is normally available to indicate when the transmitter is starting to transmit a pulse and therefore occurs at the PRF. This “trigger” pulse is normally used as the ECDR-814x “Trigger Input,” either directly or indirectly, to establish the start time for receiver data collection. The I and Q sample pairs are written to FIFO.

An example of indirect usage involves using the “trigger” pulse to produce a delayed output pulse, which in turn becomes the input Trigger signal. If such a delay is programmable, then the start of data collection can be varied in time, which for radar, would correspond to a variable delay in range from the radar. Similarly, applications such as MRI, can employ a fixed delay to provide a receiver “blanking” interval, which essentially “disables” the receiver during the time of pulse transmission. As a result, only true “return” data for that pulse is processed.

Constant Phase

For coherent radar the phase of the NCO is started at the same place for each acquisition (constant phase). This is enabled on each channel by the NCO Sync Enable bit. Non-coherent MRI applications do not require the constant phase feature. However, before data is received, the processing chain is cleared for both coherent and non-coherent applications.

When the signal trigger occurs, the receiver starts processing the current A/D sample and outputs the result to the FIFO. This feature is important for MRI applications because it enables the board to capture the transient response. For instance, if you require accurate radar range determination, you must place the trigger activating edge relative to the A/D clock.

Two modes (options) are available for controlling where data collection ends:

- Sync mode collects a programmed number (up to 128K) of I and Q sample pairs.
- Gate mode collects I and Q sample pairs for as long as the trigger signal is active.

Applications that require a known, fixed number of samples typically use the Sync mode. An exception to this is a radar application where, for a given transmitted waveform, the “range extent” for which data is to be collected, varies at a rate sufficient to preclude re-programming the appropriate receiver channel-pair data collection counter. This is the case for multiple-target tracking radar, which varies the width of the “track gate” (data collection interval) as a function of track quality (i.e., degree of uncertainty as to actual target location) for each target.

Typical CW Application Usage

CW applications require a continuous data throughput similar to those found in common wireless communications receivers. These applications typically involve wideband, multi-channel wideband, and multi-channel narrowband receiver data processing requirements of phase-modulated or frequency-modulated CW waveforms associated with radar or communications systems. For applications where there is an abrupt change, for example, a jump in frequency for

radar range determination, the application can more closely resemble the pulsed systems described in the next section.

For a CW Application, the analog input channels are digitized by AD6644 A/Ds and then routed to the two AD6620s, which can be interleaved. A single channel supports bandwidths of up to 2 MHz.

Narrow Pulse Applications

For narrow pulse (and therefore wideband) applications such as high resolution tracking radar, note that there are constraints in the number of taps the FIR filter can use before radar resolution is degraded. Typically, the number of taps times the tap spacing should not exceed twice the pulse width. For example, if the FIR is being clocked at 65 MHz (about 15.38 nanoseconds) and the transmitted pulse width is 400 nanoseconds, the maximum number of taps that can be used is 52 (i.e., $800/15.38=52$). Such applications also typically interleave the AD6620s to minimize receiver decimation for a given number of taps in support of wider bandwidth requirements.

Chapter 2 Product Overview

This chapter provides more detailed product features, including analog signal inputs, clocking, channel configurations, and A/D data.

Analog Signal Input

The ECDR-814x board is available in no gain and gain models. The no gain model enables you to collect only transformer-coupled data with the A/D data. With the gain model you can collect transformer-coupled data with the A/D data *and* also A/D data through a 20dB gain block.

No Gain

The ECDR-814x receives analog signals through the front panel SMA connectors, which are transformer coupled and are 50 Ω impedance. The analog signals then are input to the AD6644, a 14-bit, 65 MHz A/D converter. The default configuration has a full-scale input of 1.1 V_{pp} (+5 dBm) using a Mini-Circuits transformer (ADT4-6) with a 10.7 MHz low pass filter from Mini-Circuits (SCLF-10.7).

Gain

The ECDR-814x receives analog signals through the front panel SMA connectors, which are transformer coupled and have 50 Ω impedance. The analog signals then are input to the AD6644, a 14-bit, 65 MHz A/D converter. You can select between a fixed full-scale input of 1.1 V_{pp} (+5 dBm) using a Mini-Circuits transformer (ADT4-6) or a programmable gain input with a full-scale input ranging from -12dBm to 19dBm in 1dB steps.

Clock Logic

You must input the clock through the front panel SMA connector. The clock signal is buffered and distributed to all eight channels so that all channels are sampled simultaneously. Specific requirements for the clock are the following:

- -2dBm (0.5V_{pp}) to +4dBm (1V_{pp})
- 70 MHz maximum rate
- Sine Wave preferred (see below)
- 50-Ohm input

The clock is received by a Positive Emitter Coupled Logic (PECL) receiver, which is AC-coupled to the input with a 50-Ohm termination. AC coupling of the input blocks the DC voltage, enabling AC peak-to-peak voltage to be received.



The clock amplitude range is -2dBm (0.5V_{pp}) to +4dBm (1V_{pp}), but smaller levels can provide a good clock. If the input is considerably larger than +4dBm (1V_{pp}), the receiver can be damaged permanently.

The external clock is buffered and provides 1:1 clocking to all the A/D converters. This same clock is also distributed to the AD6620 digital receivers. You can choose to clock the digital receivers at the same rate or twice the rate of the A/D converters. The clock rate selection is done in groups of four channels (channels 0-4 and/or 3-7).

If the A/D converters are operated at the same rate as the receivers, the maximum clock rate is 70 MHz. However, if you are operating any of the receivers at twice the clock rate of the A/D converters, the maximum input is 35 MHz.

It is generally desirable to operate the AD6620 digital receiver clock at the highest possible rate, since this permits the largest number of filter taps to be used for a given filter design. Also, it is generally desirable to operate the A/D at the highest possible clock rate since the receiver “processing gain” is achieved through the reduction of noise bandwidth via the filtering and associated data rate decimation process. Refer to the AD6620 data sheet for more information on filter configurations.



We recommend that you use a low phase noise sine wave as a source. However, if you use a square wave, select a 50 percent duty cycle with very low jitter. Any phase noise (jitter for a square wave) on the input directly translates as distortion in the A/D converter and is reflected in the digitized data.

Channel Configurations

The ECDR-814x board supports the following data collection modes, whether you are using a 2-, 4-, or 8-channel configuration.

- Acquire raw A/D data
- Add consecutive raw A/D data samples and then average the result. The number of samples summed and then averaged can be 1, 2, 4, 8, 16, 32, 64, 128, or 256.
- Acquire and process the data through the AD6620's.
- Add consecutive data samples from the AD6620 and then average the result. The number of samples summed and then averaged can be 1, 2, 4, 8, 16, 32, 64, 128, or 256. This can only be done for one of the quadrature components.

Table 2-1 shows the configurations and the corresponding input channels available on the ECDR-814x board. For example, signals received by an ECDR-814x configured with two channels are input into channels 0 and 2. The registers for channels 0 and 2 handle the control for data collection.

The registers for channels 1 and 3 respond to VME access, but do not perform any control function. Channels 4 through 7 do not respond to VME access in a configuration of two channels.

Table 2-1 ECDR-814x Board Configuration and Input Channels

Board Configuration	Signal Input Channels
Two channels	Channels 0 and 2
Four channels	Channels 0, 2, 4, 6

Signals received by an ECDR-814x configured with four channels are input into channels 0, 2, 4, and 6. The registers for channels 0, 2, 4, and 6 handle the control for data collection. The registers for channels 1, 3, 5, and 7 respond to VME access, but do not perform any control function.

A/D Data

A channel can be configured to acquire raw A/D data with a sample rate up to 65 mega-samples per second (MSPS). The raw samples are stored in the FIFO as a 32-bit word composed of two 16-bit samples. These samples are right justified with the two least significant bits (LSB)s always set to zero so that the data can be processed as 16-bit data.

The samples can also be summed together in order to improve the signal-to-noise ratio (SNR) of the A/D data. When the samples are summed, the results are stored in the FIFO as a 32-bit number. This data is shifted so that the accumulated value can be treated the same no matter the number of accumulated samples. The channel can accumulate 1, 2, 4, 8, 16, 32, 64, 128, or 256

samples. For more information on combining samples, refer to “Data Format” in *Chapter 5 Operating Guide*.

Channel/Receiver Configurations

Each of the eight channels employs dual AD6620s to permit decimation in the Finite Impulse Response (FIR); however, a single channel can use one or two AD6620 Digital Receiver chips. A single AD6620 per channel provides sufficient processing capability for narrow bandwidth applications, while the use of dual AD6620's per channel provides equivalent performance for applications requiring up to twice the bandwidth. More specifically, the number of taps required for adequate FIR filter performance essentially determines the bandwidth that can be supported by a single AD6620. Follow these guidelines if your application requires both the AD6620s:

- Number of FIR Taps must be even.
- Decimation of the FIR must be even.
- Max FIR Taps \leq (Total Decimation of one AD6620) x (# of AD6620s) x (Ratio of AD6620 clock to the A/D clock)

For example, with two AD6620s, each with a total decimation of 64, and the AD6620s operating at twice the A/D clock rate, the maximum number taps available for the FIR is 256.

When two AD6620's are used, they are operated the same but the FIR section of the second AD6620 is started after the first AD6620 FIR section has processed one half the number of taps. Thus, the samples are output as follows:

I and Q from the first AD6620
I and Q from the second AD6620
I and Q from the first AD6620
And so on...

The receiver's complex sample pair can be output to the FIFO; however, the channel can be set up to accumulate either one of the quadrature components. This accumulation can be 1, 2, 4, 8, 16, 32, 64, 128 or 256 samples when either one or two AD6620s are used.

Data Acquisition Modes

The ECDR-814x has been designed to support data acquisition for both CW and pulsed system applications. An SMA connector external sync input on the front panel supports two operating modes: Trigger mode, which collects data with each occurrence of an external trigger pulse; and Gate mode, which provides control of the data processing interval based on an external signal.

An input connector is provided to enable the insertion of a 16-bit wide digital header word into the data stream or for tagging data. This word is latched in on the rising edge of the sync signal and is available for you to read as needed.

Gate Mode

In addition to the Trigger mode, the ECDR-814x provides a Gate mode where you can input an external signal to control the data collection. In the Gate mode, data is collected as long as the Gate signal is active; however, data can be lost if you can not move the data out of the FIFO faster than it is being generated.

Trigger Mode

The Trigger mode treats the external trigger input or the Software Sync Bit like a synchronizing “trigger.” With the Free Run bit set to “0” the rising edge of the trigger initiates the collection of a software-programmed number of data samples. Note that the programmable counter is 17 bits wide, permitting collection of up to 128K sample pairs, which is the maximum depth of the FIFOs. If the Free Run bit is set to “1,” then data collection begins when the external trigger is received and continues until the Trigger Clear bit is written. Data can be lost if it can not move out of the FIFO faster than it is being generated.

Depending on the number of AD6620s used per channel and the resultant decimation, the hardware automatically accounts for any internal delays. Since the delays are accounted for, the first I and Q sample pair collected (written to FIFO) corresponds to the first valid output for receiver processing starting with the first A/D data input following that trigger Input rising edge. This is possible because the AD6620 CIC and FIR sections are essentially cleared by the occurrence of the trigger input. They begin calculating at the next A/D input sample. You also have the option to reset the AD6620 NCO with each trigger to provide a zero start phase or any other start phase. However, the AD6620 phase offset register must be programmed to that desired phase, rather than zero, to support pulsed coherent systems.

Chapter 3 Specifications

This chapter provides the following specifications for the ECDR-814x board:

- General Specifications
- Power Requirements
- Environmental Specifications

General Specifications

Physical Specifications

Size	VME 6U
Interface	VME64X Only

Connector Specifications

Input connector	Coax Type SMA
Header words	AMP 104066-1 (mating connector 111196-4)

Power Requirements (typical)

Configuration	+5Vdc	+3.3Vdc	+12Vdc	-12Vdc	Power
ECDR-814/8	4.8A	1.9A	NA	NA	31W
ECDR-814/4			NA	NA	
ECDR-814/2			NA	NA	
ECDR-814/8-AD			NA	NA	
ECDR-814/4-AD			NA	NA	
ECDR-814/2-AD	3.6A	0.3A	NA	NA	19W
ECDR-814G/8	5.6A	2.4A	0.66A	8 μ A	44W
ECDR-814G/4				4 μ A	
ECDR-814G/2				2 μ A	
ECDR-814G/8-AD				8 μ A	
ECDR-814G/4-AD				4 μ A	
ECDR-814G/2-AD				2 μ A	

Environmental Specifications

Parameter	Operating	Storage
Temperature	0- 55 ° C	-55 °C - + 100 °C
Relative Humidity	95% Non-Condensing	95% Non-Condensing
Cooling Requirement	A Linear Air Flow of > 2.5 Meters/sec is recommended.	N/A
Thermal Shock	5 °C/MIN	10 ° C/Min
Altitude	-1000 – 10000 Feet	-1000 – 50000 Feet
Vibration	10 to 100 HZ @ 2G	10 to 500 HZ @ 2G
MTBF	> 100,000 Hours	N/A
Mechanical Shock	20G for 6 MS (Half Sine) when mounted in a suitable racking system	

Chapter 4 Installation and Setup

This chapter provides board installation and setup information, including setting switches and connectors.

Unpacking the Product



Before unpacking the product, note the following guidelines:

- Check the shipping carton for damage. If the product's shipping carton is damaged upon arrival, request that the carrier's agent be present during unpacking and inspection of module(s).
- Make sure that the area designated for unpacking the product is a static electricity-controlled environment.
- Unpack the ECDR-814 board *only* on a grounded conductive pad using an anti-static wrist strap grounded to the pad.
- If moving the board is necessary, move it in an ESD protective container.

Note: The ECDR-814 board is shipped in an ESD protective container.

- Always avoid touching areas of integrated circuitry as static discharge can damage circuits.



After unpacking the product, check the contents of the container against the packing slip to verify that all items are present and undamaged.

ECDR-814x Board Switches

The switches provided on the ECDR-814 board are as follows:

- S1 – Enables you to bypass the VME Bus Grant signals; these signals are normally off.
- S2 – Sets the VME Bus request, which is used when the ECDR-814x is the bus master.
- S3 – Controls the VME Bus Interrupt Level, used by the ECDR-814x when interrupts are enabled.
- S4 – Sets the base address of the ECDR-814x in the VME Bus A32 address space.
- S5 – Selects the Raceway Bus Clock. The switch is set to match the clock rate provided by the Raceway back plane. This enables the Racelink to properly generate the Raceway timeout.

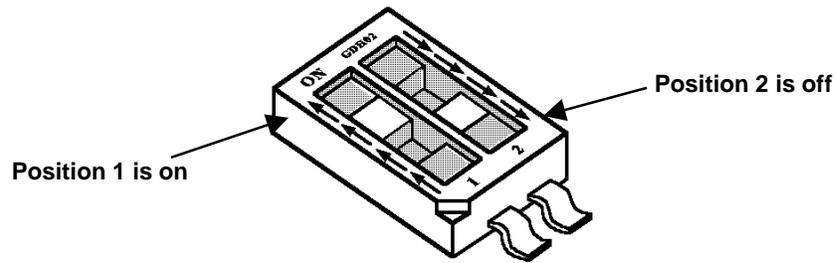


Figure 4-1 Setting Switches on the ECDR-814x

As shown above, enable the **ON** position by pushing the slider towards the side of the switch where the word **ON** is printed. To enable the **OFF** position, push the slider away from the side of the switch where the word **ON** is printed.

Note: In the event that the word *ON* has been rubbed off, remember that the ON position is on the opposite side of the beveled corner.

Setting Switches

Set the S1 through S5 switches on the ECDR-814 board as shown in the following tables.

S1 - Bus Grant Daisy Chain 0 through 3 Bypass	Pos 4	Pos 3	Pos 2	Pos 1
Bus Grant 0 Bypass	off	off	off	off
Bus Grant 1 Bypass	off	off	on	off
Bus Grant 2 Bypass	off	on	off	off
Bus Grant 3 Bypass	on	off	off	off

S2 - Bus Request 0 through 3	Pos 2	Pos 1
Level 0 Selected	on	on
Level 1 Selected	on	off
Level 2 Selected	off	on
Level 3 Selected	off	off

S3 - Interrupt Level and VME DMA Interleave Enable (switch is read at power-up only)	Pos 4	Pos 3	Pos 2	Pos 1
No Interrupt	X	on	on	on
Interrupt Level 1 Select	X	on	on	off
Interrupt Level 2 Select	X	on	off	on
Interrupt Level 3 Select	X	on	off	off
Interrupt Level 4 Select	X	off	on	on
Interrupt Level 5 Select	X	off	on	off
Interrupt Level 6 Select	X	off	off	on
Interrupt Level 7 Select	X	off	off	off
VME DMA Interleave Enable	off	X	X	X
VME DMA Interleave Disable	on	X	X	X

S4 - Base Address		
Position	Address Bit	Example Address Setting 0Dxxxxxx
8	A31	On - (0)
7	A30	On - (0)
6	A29	On - (0)
5	A28	On - (0)
4	A27	Off - (1)
3	A26	Off - (1)
2	A25	On - (0)
1	A24	Off - (1)

S5 - Raceway Bus Clock	Pos 1	Pos 2
Raceway Clock 40MHz	On	X
Raceway Clock 66.6MHz	Off	X

Connectors

Input Connectors

Connector	Function 8 Channel Configuration	Function 4 Channel Configuration	Function 2 Channel Configuration
J1A	Channel 0 Input (SMA)	Channel 0 Input (SMA)	Channel 0 Input (SMA)
J1B	Channel 1 Input (SMA)	NA	NA
J1C	Channel 2 Input (SMA)	Channel 2 Input (SMA)	Channel 2 Input (SMA)
J1D	Channel 3 Input (SMA)	NA	NA
J1E	Channel 4 Input (SMA)	Channel 4 Input (SMA)	NA
J1F	Channel 5 Input (SMA)	NA	NA
J1G	Channel 6 Input (SMA)	Channel 6 Input (SMA)	NA
J1H	Channel 7 Input (SMA)	NA	NA
J2	External Clock Input (SMA)	External Clock Input (SMA)	External Clock Input (SMA)
J3	External Sync Input (SMA)	External Sync Input (SMA)	External Sync Input (SMA)
J4	Header Input	Header Input	Header Input

Header Input (J4) Pin Functions

Logic 1: 2 to 5.5 Vdc

Logic 0: -0.5 to 0.8 Vdc

Pin	Function
1	Ground
2	Ground
3	Header Bit 0
4	Header Bit 1
5	Header Bit 2
6	Header Bit 3
7	Header Bit 4
8	Header Bit 5
9	Header Bit 6
10	Header Bit 7
11	Header Bit 8
12	Header Bit 9
13	Header Bit 10
14	Header Bit 11
15	Header Bit 12
16	Header Bit 13
17	Header Bit 14
18	Header Bit 15
19	Ground
20	Ground

Chapter 5 Operating Guide

This chapter provides information for connecting inputs to signal sources, configuring the VME Bus and the AD6620s, and synchronizing operation and control. This chapter also includes examples of data collection.

Connecting to the IF Inputs

After installing the ECDR-814x, connect the IF inputs to the signal source. Read these guidelines carefully before you begin.

- Check for proper signal level. The IF inputs can accept a signal of up to $\pm 0.56\text{Vp}$ Max (+5 dBm).



The input impedance is 50 Ohms. The signal source must be able to drive the impedance to the required signal level. A signal level greater than $\pm 0.56\text{Vp}$ Max (+5 dBm) saturates the A/D and can damage the A/D converters. The maximum signal that will not damage the A/D converters is $\pm 1.1\text{Vp}$; however, this signal will prevent the A/D converter from outputting valid data.

- If the signal level is unacceptable (greater than +5 dBm), use an in-line 50-ohm attenuator to drop the signal level to an acceptable level.
- If you did not order filtering on your ECDR-814x, use an in-line 50 ohm, anti-alias filter, either a low pass or a band pass filter. Note that there is no filtering on the I/F inputs of the ECDR-814Gx. Your choice of anti-alias filter depends upon the intended application. If you do not use a filter, the A/D converters digitize signals from 150 KHz up to 250 MHz for the ECDR-814x, and 2 MHz up to 300 MHz for the ECDR-814Gx, with little or no attenuation. Signals outside this band will also be digitized, but at various attenuated levels.
- Use a high quality cable with matched 50-Ohm characteristic impedance; make sure the source is shielded and has a good ground connection. Using high quality cable is important to prevent very small and undesired signals and noise from being “picked up” by the cable.
- Correctly ground the complete system. To prevent the introduction of noise to the A/D converters, ensure that no ground differences exist between the source and the ECDR-814x.
- Use an SMA adapter to the required cable type or an SMA-type cable to connect the inputs.

Connecting to the Clock Input

After you have connected the IF inputs to the signal source, connect the clock signal source to the clock input. Read these guidelines carefully before you begin.

- Check the clock source for proper signal level. The signal level should be within an input range of -2 dBm to +4 dBm. The source must be able to drive the input impedance of 50 Ohms to the minimum input level. The minimum signal that can be received correctly is $\pm 0.25\text{Vp}$ (-2 dBm).
- We recommend that you use a low phase noise sine wave as a source. However, if you use a square wave, select a 50 percent duty cycle with very low jitter.



Any phase noise (jitter for a square wave) on the input directly translates as distortion in the A/D converter and is reflected in the digitized data.

- Use an SMA adapter to the required cable type or an SMA-type cable to connect the clock inputs.

Connecting to the Gate/Trig Input

After connecting the clock signal source to the clock input, connect the signal source to the Gate/Trig input. Read these guidelines carefully before you begin.

- Use a TTL level input signal. The input impedance is 1K Ohms, which for most sources is high impedance. If you are connecting a 50-Ohm source, halve the output voltage you would normally use. For example, if 0V to 3V is the required signal level, set the signal generator output to 0V to 1.5V.
- Use a square wave input with fast rise and fall times of about 5nSec. This input operates optimally when it is synchronized with the input clock and meets the setup and hold times as specified in Chapter 3 Specifications.

For counted burst applications, this input is a pulse, and must be at least one input clock wide. For continuous gate applications, this input can be any size above one of the receiver output clocks (the decimated clock rate that the receiver channels will output). For example if the input clock is 65 MHz, and the total receiver decimation is 16, then a minimum gate width of 246nSec should be used (the output clock rate is $65 \text{ MHz}/16 = 4.06 \text{ MHz}$; the clock period = 246nSec).



When Gate/Trig input is not synchronous with the input clock, jitter is introduced on the Gate/Trig signal dependent upon the input clock period (+/- 1 clock of jitter). The jitter only pertains when the collection is started and not to the sample clock.

Data Collection Modes

This section provides instructions for configuring and initializing the ECDR-814x for the three data collection modes: Gate Continuous, Free Run, and Counted Burst. Before you perform these operations, however, you should decide on the appropriate collection mode for your product application. Table 5-1 provides a list of options you should consider, including the number of channels to be used, type of data, signal source, and synchronization method. Table 5-2 lists a general order in which registers should be written to perform data acquisition.

Table 5-1 Selecting a Data Collection Mode

Configuration Items	Options
Collection Mode	Gate Continuous Free Run Counted Burst
Channels	1 2 4 8
Type of Collection Data	A/D Data <ul style="list-style-type: none"> ▪ Raw Data ▪ Accumulated Data Receiver Data (single or dual receivers) <ul style="list-style-type: none"> ▪ Complex Data ▪ Accumulated I Data ▪ Accumulated Q Data Test Counter Data
Gate/Trigger Source	External Gate/Trig Input Register Control

Table 5-2 General Initialization

Order	Operation	Result
1	Write 1 to bit 12 of the Command/Status Register (CSR).	Clears the ECDR-814x.
2	Read Interrupt Status (INTSTAT).	Clears Interrupt Status.
3	Write the CSR.	General configuration for the ECDR-814x. If changing bits 7, 8, or 17-20, delay for 15mS after writing this register to allow for the clock to stabilize.
4	Write the interrupt vector register if interrupts are used.	Configures the ECDR-814 with a unique interrupt vector to be used to distinguish the board if interrupts are used.
5	Write Interrupt Mask Register.	Enables the interrupts if any are used.
6	Write the Command / Status Register for each of the channel pair (four total).	Configures each pair of channels with general requirements.
7	Write the Receiver Decimation Register (RDEC) for each channel.	Configures the control logic with the correct settings. Only needs to be written when using 2 receivers on one channel.
8	Write the Receiver Control Channel Register (RCTL) for each channel.	Selects the type of data selected, the numbers of samples accumulated, the trigger mode, and the burst counter MSB.
9	Write the Data Window Size Register for each channel if using the Counted Burst mode. (The MSB is in the RCTL register).	Determines the amount of data collected when operating in the Counted Burst Mode.
10	Write the Gain register with appropriate gain if using the ECDR-814G/x	Sets the gain for the specific channel.
11	Configure the AD6620 registers if acquiring receiver data.	Sets up your user-specific requirements in the digital receivers.

Configuring the AD6620

You must configure each of the AD6620s Digital Receivers prior to collecting receiver data. Since all of the registers in the AD6620s are 32-bit wide, you perform two 16-bit reads or writes accessing the first address given, followed by the second address. For example, when accessing the Mode Control Register you must access offset 1800, then 1804. The value in 1800 is the least significant word and the value 1804 is the most significant word. If the registers are not accessed in order, the incorrect data is read or written to the AD6620s.

For the ECDR-814x you write the Mode Control register to zero before configuring the AD6620 digital receivers. Once this is done the registers can be written in any order with your application-specific configuration.

Getting Data: Complete Collection Examples

This section provides examples of the following data collection modes and basic channel configurations for the ECDR-814x board:

- Counted Burst, Eight-Channel, Raw A/D Data
- Free Run, Four-Channel, Single Receiver Data
- Gate Continuous, One-Channel, Dual Receiver Data

These examples give you an overview of how to use the board to collect data and provide a starting point for developing your specific applications.

Counted Burst, Eight-Channel Raw A/D Data Application

The Counted Burst, Eight-Channel Raw A/D data collection is initiated by a register write and is terminated when the burst counter expires. The expiration of the burst counter is signaled by a VME interrupt.

The table below provides setup information for collecting eight-channel, raw A/D data, which you can use to develop a template for your specific applications. After completing the setup, connect the input signal to IF Input for Channel 0 and the Clock to the Clock input. With this configuration, the signal is digitized on channel 0 and all the other channels digitize a noise floor.

Test Setup Hardware	Description
IF Input Source: RF Signal Generator	Amplitude = +4dBm, Frequency = 2.5 MHz. Signal Generator should be as good as is available (for example, minimum distortion, harmonics, and phase noise).
Low Pass Filter	Fc = 3 MHz to 4 MHz, as good as available.
High Pass Filter	Fc = 1 MHz to 2 MHz, as good as available.
Clock Source: RF Signal Generator	Amplitude = +4dBm Frequency = 64.8 MHz. Signal Generator should be as good as is available (for example, minimum distortion, harmonics, and phase noise).
BNC Cables	Good quality BNC Male to BNC Male cables.
BNC to SMA Adapters	BNC Female to SMA Male adapters.

Counted Burst Data Collection Sequence

The following table provides the sequence of events for the Counted Burst, Eight-Channel Raw A/D data collection mode. Ensure that the switches are in a usable state prior to beginning. Refer to Chapter 6 Register Maps for more information.

Order	Operation	Effect
1	Write 1 to bit 12 of the Command/Status Register (CSR).	Clears the ECDR-814x.
2	Read Interrupt Status (INTSTAT).	Clears Interrupt Status.
3	Write the CSR with 8Ah, then delay 15mS for the PLL to stabilize.	Configures the board to read eight channels and sets the PLL to high range corresponding to the 64.8MHz clock.
4	Write the Interrupt Vector with EDh (or any value your system can handle).	Configures the ECDR-814 with a unique interrupt vector to be used to distinguish the board.
5	Write 001h to the Interrupt Mask Register.	Enables generation of an interrupt when the Channel 0 Burst Counter expires. The interrupt also indicates that channels 1-7 have data because all the channels will be configured the same for this example.
6	Write 1Ch to the Command/Status Register for each channel pair.	Programs the FIFO Flags with the appropriate value to optimize throughput for eight-channel mode.
7	Write a 16h to the Receiver Control Channel Register for each channel.	Configures the channel to collect Raw Data and enables the Trigger mode.
8	Write 3FFh to the Data Window Size Channel Register	Enables the board to collect 1024 words (or 2048 samples) per channel. Different values can be written for a different data set size.
9	If using an ECDR-814Gx, write 0h to the Gain Channel Register for each of the channels	Configures the IF input with no additional gain.
10	Read the Command /Status Register. Write the value read ORed 800h back to the register.	Issues a software trigger to the board without changing the contents of the Command / Status Register.

Counted Burst Data Collection Sequence (continued)

Order	Operation	Effect
11	An interrupt is generated from the board with the Interrupt Vector EDh (or the value programmed earlier). A read of the Interrupt Status Register with FFh indicates that all channels have data in the FIFO. This read also clears the interrupt.	Interrupt indicating the data is available.
12	Read address offset 10 0000h and subsequent addresses for data (you can just read from the 10 0000h only or increment the address on each read to obtain data).	By the way the example was configured there are 8192 words available. See Table x-x for data format. There are several ways to read the data from this address: your CPU can DMA data, the on board DMA controller can move the data (see section x.x), or the Raceway can move the data (see section x.x).
13	After all the data is read, repeat steps 10-12	Takes another data set.

Free Run, Four-Channel Single Receiver Data Application

The Free Run, Four-Channel Single Receiver data collection is initiated by a register write and continues until you issue a trigger clear command.

After you set the input signal to 5.92 MHz, the signal is digitized and down converted by 5.8887 MHz, and then filtered. The filtering decimates the data by a factor of 256 for a bandwidth of 253 kHz. The resulting signal is at 31.3 kHz.

The table below provides setup information for collecting four channels of single receiver data, which can be used to develop a template for your specific applications. After completing the setup, connect the input signal to IF Input for Channel 0 and the Clock to the Clock input. With this configuration, the signal is digitized on channel 0 and all the other channels digitize a noise floor.

Test Setup Hardware	Description
IF Input Source: RF Signal Generator	Amplitude = +1dBm, Frequency = 5.92 MHz. Signal Generator should be as good as is available (for example, minimum distortion, harmonics, and phase noise).
Low Pass Filter	Fc = 7 MHz to 10 MHz, as good as available.
High Pass Filter	Fc = 1 MHz to 2 MHz, as good as available.
Clock Source: RF Signal Generator	Amplitude = +4dBm, Frequency = 64.8 MHz. Signal Generator should be as good as is available (for example, minimum distortion, harmonics, and phase noise).
BNC Cables	Good quality BNC Male to BNC Male cables.
BNC to SMA Adapters	BNC Female to SMA Male adapters.

Free Run Data Collection Sequence

The table below provides the sequence of events for Free Run, Four-Channel Single Receiver data collection. Ensure that the switches are in a usable state prior to beginning. Refer to Chapter 6 Register Maps for more information.

Order	Operation	Effect
1	Write 1 to bit 12 of the Command/Status Register (CSR).	Clears the ECDR-814x.
2	Read Interrupt Status (INTSTAT).	Clears Interrupt Status.
3	Write the CSR with 8Ah then delay 15mS for the PLL to stabilize.	Configures the board to read eight channels and sets the PLL to high range corresponding to the 64.8MHz clock.
4	Write the Interrupt Vector with EDh (or any value your system can handle).	Configures the ECDR-814 with a unique interrupt vector to be used to distinguish the board.
5	Write 600h to the Interrupt Mask Register.	Generates an interrupt when the Raceway is done with a DMA set.
6	Write 1Ah to the Command / Status Register for each channel pair.	Programs the FIFO Flags with the appropriate value to optimize throughput for four channel mode. This operation also sets the NCO Sync Enable to allow the NCO in the ADD6620 to be started at 0 phase when the trigger is received.
7	Write a 211h to the Receiver Control Channel Register for each even channel (0, 2, 4, & 6).	Configures the channel to collect Single Receiver data, free run mode, and enables the Trigger mode.
8	If using an ECDR-814Gx then write 0h to the Gain Channel Register for each of the even channels.	Configures the IF input with no additional gain.
9	Configure the Receiver as shown in Table 5-3.	Configures the receiver with the filters for this example.
10	Start the Raceway DMA with as large as possible a DMA. The local address offset for data will be 10 0000h.	Initiates the Raceway looking for data to be available from the digital receivers and continues looking until all data is moved.
11	Read the Command /Status Register. Write the value read ORed 800h back to the register.	Issues a software trigger to the board without changing the contents of the Command/Status Register. It starts moving out the Raceway since the Raceway was initiated in the previous step.

Free Run Data Collection Sequence (continued)

Order	Operation	Effect
12	An interrupt is generated from the board with the Interrupt Vector EDh (or the value programmed earlier). A read of the Interrupt Status Register with 200h indicating that the Raceway has finished moving its current DMA. Restart the DMA as soon as possible by repeating step x.	Interrupt indicating one DMA is complete. Continue steps 10 and 12 for additional data collection.
13	When you are ready to stop data collection, write an 801Ah to the Receiver Control Register for each even channel.	Issues a Trigger Clear command. It is best to wait until the DMA interrupt is generated in step 12 so that the Raceway is stopped in a known state. Otherwise a complete reset is required to restart acquisition.
14	Issue 180Ah to the Command/Status Register Channel for each channel pair.	Clears the FIFO for each channel. Restart the DMA by performing steps 10-12.

Gate Continuous, One Channel Dual Receiver Data Application

The setup for Gate Continuous, One-channel Dual Receiver data collection is the same as the single receiver example but uses two receivers to increase the bandwidth of the data collection to 506 kHz. The resultant signal transmits at 31.3 kHz. The external gate controls the data collection.

The setup information in the table below enables you to collect one channel of dual receiver data; you can use this setup as a template for your specific applications. After completing the setup, connect the input signal to IF Input for Channel 0 and the Clock to the Clock input. With this configuration, the signal is digitized on channel 0; all the other channels digitize a noise floor.

Test Setup Hardware	Description
IF Input Source: RF Signal Generator	Amplitude = +1dBm, Frequency = 5.92 MHz. Signal Generator should be as good as is available (for example, minimum distortion, harmonics, and phase noise).
Low Pass Filter	Fc = 7 MHz to 10 MHz, as good as available.
High Pass Filter	Fc = 1 MHz to 2 MHz, as good as available.
Clock Source: RF Signal Generator	Amplitude = +4dBm, Frequency = 64.8 MHz. Signal Generator should be as good as is available (for example, minimum distortion, harmonics, and phase noise).
Gate/Trig Source	Configure the Gate as shown in the <i>Connecting to the Gate/Trig Input</i> section. The Gate should be 2.1mS wide.
BNC Cables	Good quality BNC Male to BNC Male cables.
BNC to SMA Adapters	BNC Female to SMA Male adapters.

Gate Continuous Data Collection Sequence

The table below provides the sequence of events for Gate Continuous, One-channel Dual Receiver data collection. Ensure that the switches are in a usable state prior to beginning. Refer to Chapter 6 Register Maps for more information.

Order	Operation	Effect
1	Write 1 to bit 12 of the Command/Status Register (CSR).	Clears the ECDR-814x.
2	Read Interrupt Status (INTSTAT).	Clears Interrupt Status.
3	Write the CSR with 280h then delay 15mS for the PLL to stabilize.	Configures the board to read channel 0, sets the PLL to high range corresponding to the 64.8MHz clock, and enables the Gate input.
4	Write 000h to the Interrupt Mask Register.	Prevents interrupts from being generated.
5	Write 12h to the Command/Status Register for channel 0 and 1.	Programs the FIFO Flags with the appropriate value to optimize throughput for one channel mode. This operation also sets the NCO Sync Enable which enables the NCO in the ADD6620 to be started at 0 phase when the trigger is received.
6	Write 7Fh to the Receiver Decimation Register for channel 0.	This value was determined first by using the decimation for one of the AD6620s, 256, and then by using the formula given for this register. See the RDEC_Cx register.
7	Write a 100h to the Receiver Control Channel Register for each channel.	Configures the channel to collect Dual Receiver data and enables the Gate mode.
8	If you are using an ECDR-814Gx, write 0h to the Gain Channel Register for channel 0.	Configures the IF input with no additional gain.
9	Configure the Receiver as shown in Table 5.3 for channel 0.	Configures the Receiver with the filters for this example.
10	Apply the 2.1mS gate	Collects approximately 1063 complex sample pairs of data.
11	Once you are sure the gate is complete, read address offset 10 0000h and subsequent addresses for data (you can read from the 10 0000h only or increment the address on each read to obtain data).	By the way the example was configured there are at least 1024 words available. See "Data Format" in this chapter. The data can be moved over the VME or the RACEway. See the <i>CYC960 and CYC961 Users Guide</i> for the details on the VME DMA and the <i>RACE++ Product Specification</i> for details on the RACEway DMA.

Gate Continuous Data Collection Sequence (continued)

Order	Operation	Effect
12	After all the data is read, write an 802h to the Command / Status register for Channel 0 and 1.	Resets the FIFO for channel 0. This reset removes any data left over following the read.
13	Repeat steps 10-12.	Takes another data set.

Configuring the AD6620 Digital Receivers

Table 5-3 provides information for configuring the AD6620 Digital Receivers for the examples included in this manual.

Table 5-3 AD6620 Digital Receiver Registers

Register (Address Offset)	Value (in hex)	Description
1800h & 1804h	0000 0000	Mode Control Register – Clears Reset and Sync Slave Mode
1808h & 180Ch	0000 0000	Enables the NCO, disables Phase and Amplitude Dither
1810h & 1814h	FFFF FFFF	NCO sync mask – set per the AD6620 data sheet
1818h & 181Ch	E8BE 22A3	Set for a down convert frequency of 5.887 MHz with a sample rate of 64.8 MHz.
1820h & 1824h	0000 0000	NCO Phase Offset when trigger is received.
1828h & 182Ch	0000 0002	CIC2 Scale Factor of 2
1830h & 1834h	0000 0001	CIC2 Decimation of 2 (value 2 – 1)
1838h & 183Ch	0000 0013	CIC5 Scale Factor of 19
1840h & 1844h	0000 001F	CIC5 Decimation of 32 (value is 32 – 1)
1848h & 184Ch	0000 0004	Output RCF Scale Factor of 4
1850h & 1854h	0000 0003	RCF Decimation of 4 (value is 4 – 1)
1858h & 185Ch	0000 0000	RCF Address Offset – This is the address offset that the RCF coefficients in the AD6620 start.
1860h & 1864h	0000 007F	Number taps used in the RCF.
1868h & 186Ch	0000 0000	Reserved register which must be written to 00h
0000h & 0004h	000F FFFF	RCF Coefficient
0008h & 000Ch	000F FFFC	RCF Coefficient
0010h & 0014h	000F FFFB	RCF Coefficient
0018h & 001Ch	000F FFF8	RCF Coefficient
0020h & 0024h	000F FFFB	RCF Coefficient
0028h & 002Ch	0000 0003	RCF Coefficient
0030h & 0034h	0000 0013	RCF Coefficient

Table 5-3 AD6620 Digital Receiver Registers (continued)

Register (Address Offset)	Value (in hex)	Description
0038h & 003Ch	0000 0025	RCF Coefficient
0040h & 0044h	0000 0031	RCF Coefficient
0048h & 004Ch	0000 0028	RCF Coefficient
0050h & 0054h	0000 0004	RCF Coefficient
0058h & 005Ch	000F FFC3	RCF Coefficient
0060h & 0064h	000F FF78	RCF Coefficient
0068h & 006Ch	000F FF42	RCF Coefficient
0070h & 0074h	000F FF4C	RCF Coefficient
0078h & 007Ch	000F FFB4	RCF Coefficient
0080h & 0084h	0000 0079	RCF Coefficient
0088h & 008Ch	0000 016A	RCF Coefficient
0090h & 0094h	0000 022B	RCF Coefficient
0098h & 009Ch	0000 0248	RCF Coefficient
00A0h & 00A4h	0000 016A	RCF Coefficient
00A8h & 00ACh	000F FF87	RCF Coefficient
00B0h & 00B4h	000F FD0D	RCF Coefficient
00B8h & 00BCh	000F FAD9	RCF Coefficient
00C0h & 00C4h	000F FA02	RCF Coefficient
00C8h & 00CCh	000F FB6D	RCF Coefficient
00D0h & 00D4h	000F FF51	RCF Coefficient
00D8h & 00DCh	0000 04E5	RCF Coefficient
00E0h & 00E4h	0000 0A5C	RCF Coefficient
00E8h & 00ECh	0000 0D5B	RCF Coefficient
00F0h & 00F4h	0000 0BD0	RCF Coefficient
00F8h & 00FCh	0000 04EC	RCF Coefficient
0100h & 0104h	000F F9E5	RCF Coefficient
0108h & 010Ch	000F EE04	RCF Coefficient

Table 5-3 AD6620 Digital Receiver Registers (continued)

Register (Address Offset)	Value (in hex)	Description
0110h & 0114h	000F E5E8	RCF Coefficient
0118h & 011Ch	000F E5F3	RCF Coefficient
0120h & 0124h	000F F06A	RCF Coefficient
0128h & 012Ch	0000 03F1	RCF Coefficient
0130h & 0134h	0000 1B23	RCF Coefficient
0138h & 013Ch	0000 2DB7	RCF Coefficient
0140h & 0144h	0000 331C	RCF Coefficient
0148h & 014Ch	0000 25DB	RCF Coefficient
0150h & 0154h	0000 0681	RCF Coefficient
0158h & 015Ch	000F DCE5	RCF Coefficient
0160h & 0164h	000F B6C6	RCF Coefficient
0168h & 016Ch	000F A3D1	RCF Coefficient
0170h & 0174h	000F AFF8	RCF Coefficient
0178h & 017Ch	000F DDFE	RCF Coefficient
0180h & 0184h	0000 2446	RCF Coefficient
0188h & 018Ch	0000 6DAC	RCF Coefficient
0190h & 0194h	0000 9ED7	RCF Coefficient
0198h & 019Ch	0000 9EFB	RCF Coefficient
01A0h & 01A4h	0000 6192	RCF Coefficient
01A8h & 01ACh	000F EDB9	RCF Coefficient
01B0h & 01B4h	000F 604D	RCF Coefficient
01B8h & 01BCh	000E E71D	RCF Coefficient
01C0h & 01C4h	000E B5C1	RCF Coefficient
01C8h & 01CCh	000E F6C6	RCF Coefficient
01D0h & 01D4h	000F BD78	RCF Coefficient
01D8h & 01DCh	0000 FCC3	RCF Coefficient
01E0h & 01E4h	0002 867D	RCF Coefficient

Table 5-3 AD6620 Digital Receiver Registers (continued)

Register (Address Offset)	Value (in hex)	Description
01E8h & 01ECh	0004 1422	RCF Coefficient
01F0h & 01F4h	0005 5707	RCF Coefficient
01F8h & 01FCh	0006 0BD6	RCF Coefficient
0200h & 0204h	0006 0BD6	RCF Coefficient
0208h & 020Ch	0005 5707	RCF Coefficient
0210h & 0214h	0004 1422	RCF Coefficient
0218h & 021Ch	0002 867D	RCF Coefficient
0220h & 0224h	0000 FCC3	RCF Coefficient
0228h & 022Ch	000F BD78	RCF Coefficient
0230h & 0234h	000E F6C6	RCF Coefficient
0238h & 023Ch	000E B5C1	RCF Coefficient
0240h & 0244h	000E E71D	RCF Coefficient
0248h & 024Ch	000F 604D	RCF Coefficient
0250h & 0254h	000F EDB9	RCF Coefficient
0258h & 025Ch	0000 6192	RCF Coefficient
0260h & 0264h	0000 9EFB	RCF Coefficient
0268h & 026Ch	0000 9ED7	RCF Coefficient
0270h & 0274h	0000 6DAC	RCF Coefficient
0278h & 027Ch	0000 2446	RCF Coefficient
0280h & 0284h	000F DDFE	RCF Coefficient
0288h & 028Ch	000F AFF8	RCF Coefficient
0290h & 0294h	000F A3D1	RCF Coefficient
0298h & 029Ch	000F B6C6	RCF Coefficient
02A0h & 02A4h	000F DCE5	RCF Coefficient
02A8h & 02ACh	0000 0681	RCF Coefficient
02B0h & 02B4h	0000 25DB	RCF Coefficient
02B8h & 02BCh	0000 331C	RCF Coefficient

Table 5-3 AD6620 Digital Receiver Registers (continued)

Register (Address Offset)	Value (in hex)	Description
02C0h & 02C4h	0000 2DB7	RCF Coefficient
02C8h & 02CCh	0000 1B23	RCF Coefficient
02D0h & 02D4h	0000 03F1	RCF Coefficient
02D8h & 02DCh	000F F06A	RCF Coefficient
02E0h & 02E4h	000F E5F3	RCF Coefficient
02E8h & 02ECh	000F E5E8	RCF Coefficient
02F0h & 02F4h	000F EE04	RCF Coefficient
02F8h & 02FCh	000F F9E5	RCF Coefficient
0300h & 0304h	0000 04EC	RCF Coefficient
0308h & 030Ch	0000 0BD0	RCF Coefficient
0310h & 0314h	0000 0D5B	RCF Coefficient
0318h & 031Ch	0000 0A5C	RCF Coefficient
0320h & 0324h	0000 04E5	RCF Coefficient
0328h & 032Ch	000F FF51	RCF Coefficient
0330h & 0334h	000F FB6D	RCF Coefficient
0338h & 033Ch	000F FA02	RCF Coefficient
0340h & 0344h	000F FAD9	RCF Coefficient
0348h & 034Ch	000F FD0D	RCF Coefficient
0350h & 0354h	000F FF87	RCF Coefficient
0358h & 035Ch	0000 016A	RCF Coefficient
0360h & 0364h	0000 0248	RCF Coefficient
0368h & 036Ch	0000 022B	RCF Coefficient
0370h & 0374h	0000 016A	RCF Coefficient
0378h & 037Ch	0000 0079	RCF Coefficient
0380h & 0384h	000F FFB4	RCF Coefficient
0388h & 038Ch	000F FF4C	RCF Coefficient
0390h & 0394h	000F FF42	RCF Coefficient

Table 5-3 AD6620 Digital Receiver Registers (continued)

Register (Address Offset)	Value (in hex)	Description
0398h & 039Ch	000F FF78	RCF Coefficient
03A0h & 03A4h	000F FFC3	RCF Coefficient
03A8h & 03ACh	0000 0004	RCF Coefficient
03B0h & 03B4h	0000 0028	RCF Coefficient
03B8h & 03BCh	0000 0031	RCF Coefficient
03C0h & 03C4h	0000 0025	RCF Coefficient
03C8h & 03CCh	0000 0013	RCF Coefficient
03D0h & 03D4h	0000 0003	RCF Coefficient
03D8h & 03DCh	000F FFFB	RCF Coefficient
03E0h & 03E4h	000F FFF8	RCF Coefficient
03E8h & 03ECh	000F FFFB	RCF Coefficient
03F0h & 03F4h	000F FFFC	RCF Coefficient
03F8h & 03FCh	000F FFFF	RCF Coefficient

Data Format

All A/D and Receiver data is 2's complement.

One-Channel Mode Read Out

All A/D and Receiver data is 2's complement. For example, to read data as a single channel (read back mode 0h – 7h), you can set the channel's Mode Select bits for different channels as required: one channel can collect raw A/D data while another is collecting receiver data. The following three modes are available:

- A/D Data: One Channel – No Accumulate
- Receiver Data: One Channel – No Accumulate
- Accumulate – One Channel

A/D Data: No Accumulate

In this mode the Mode Select bits are set to 6h (Raw Data /No Accumulate). You can select the desired channel to read back by setting the read back mode in the CSR register.

Bit 31-16	Bit 15-0
Sample 1	Sample 0
Sample 3	Sample 2

Receiver Data: No Accumulate

In this mode the Mode Select bits are set to 2h – 5h (Receiver Data /No Accumulate). You can select the desired channel to read back by setting the read back mode in the CSR register. This mode is not applicable when the ECDR-814x is used as an A/D board.

Bit 31-16	Bit 15-0
Sample 0 – I	Sample 0 – Q
Sample 1 – I	Sample 1 – Q

Accumulate

In this mode the Mode Select bits are set to 0h, 1h, or 7h (Accumulated Data). You can select the desired channel to read back by setting the read back mode in the CSR register.

Bit 31 – 0
Sample 0
Sample 1

Header Format

If enabled, the following two-word header can be inserted in the following format prior to every 8-words read.

Note: Consult Echotek Corporation if other headers are required.

Header Format																															
3	3	2	1	1	1	1	1	1	1	1	1	1	9	8	7	6	5	4	3	2	1	0									
1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0										
Channel Out of Range (Out of Range = 1)												Packet Count (Incremented on each trigger)																			
FIFO Empty Ch 7- Ch 0 (Empty = 1)												FIFO Full Ch 7 – Ch 0 (Full = 1)								Header Word From External Connector Bit 15-0											

Chapter 6 Register Maps

This chapter provides memory maps and registers for the ECDR-814x board.

ECDR-814x Memory Map

This section includes the following register space tables:

- Baseboard Register Space
- DMA Controller Register
- Channel Register Space

Note: The RACELINK Register Space is shown in the RACE++ Product Specification, Echotek Corporation.

Table 6-1 ECDR-814x Memory Map

Address Range Offset from Base Address	Description
00 0000h to 00 7FFCh	ECDR-814x Baseboard Register Space
00 8000h to 00 FFFCh	VME 961 DMA Controller Register
01 0000h to 01 FFFCh	CH[1..0] Channel Register Space
02 0000h to 02 FFFCh	CH[3..2] Channel Register Space
03 0000h to 03 FFFCh	CH[5..4] Channel Register Space
04 0000h to 04 FFFCh	CH[7..6] Channel Register Space
05 0000h to 05 FFFCh	RACELINK Register Space
06 0000h to 0F FFFCh	Not Used
07 xxx0h	Header Word 0
07 xxx4h	Header Word 1
08 xxxh	Channel 0 data
09 xxxh	Channel 1 data
0A xxxh	Channel 2 data
0B xxxh	Channel 3 data
0C xxxh	Channel 4 data
0D xxxh	Channel 5 data
0E xxxh	Channel 6 data
0F xxxh	Channel 7 data
10 0000h to 3F FFFCh	FIFO Data Space

ECDR-814x Baseboard Register Space

This section includes tables for each Baseboard Register space.

Table 6-2 ECDR-814x Baseboard Register Space

Address Offset	Abbreviation	Register Name	Attribute
0 0000h	CSR	Command/Status Register	Read/Write
0 0004h	FLAGS	FIFO Flags	Read Only
0 0008h	INTVEC	Interrupt Vector	Read/Write
0 000Ch	INTMASK	Interrupt Mask	Read/Write
0 0010h	INTSTAT	Interrupt Status	Read Only
0 0014h	HEAD0	Header Word 0 Status	Read Only
0 0018h	HEAD1	Header Word 1 Status	Read Only

Table 6-3 Command Status Register

Abbreviation	Width	Address Offset	Mask	Attribute												
CSR	32	0 0000h	001FFFFFF	R/W												
Least Significant Word																
1 5	1 4	1 3	1 2	1 1	1 0	9	8	7	6	5	4	3	2	1	0	Description
																<p>VME Only Bit 0h = VME or RACEWAY can move data 1h = RACEWAY disabled, VME data moves only</p>
																<p>D64 2K Enable Bit This enables the VME Bus on card DMA Controller to perform D64 Block transfers and re-broadcast the address every 2K Byte boundary only, otherwise it will be every 256 Byte Boundary. 0: Disabled (default) 1: Enabled</p>
																<p>Frequency Select Bits Enables 15mS for the PLL to stabilize as changing these bits. 00 = LOW (15 MHz to 35 MHz) 01 = HIGH (40 MHz to 100 MHz) 10 = MID (25 MHz to 60 MHz) 11 = MID (25 MHz to 60 MHz)</p>
																<p>External Enable Bit 0h = Idle 1h = Opens path to accept the External SYNC pulse</p>
																<p>Receiver Clock Multiplier Channels 0-3 Enables 15mS for the PLL to stabilize as changing these bits. These are not available on the NR revision. 00 = Receiver Clock Equals AD Clock 01 = Receiver Clock 2 Times AD Clock 10 = Receiver Clock 4 Times AD Clock 11 = Receiver Clock Equals AD Clock</p>
																<p>Receiver Clock Multiplier Channels 4-7 Enables 15mS for the PLL to stabilize as changing these bits. These are not available on the NR revision. 00 = Receiver Clock Equals AD Clock 01 = Receiver Clock 2 Times AD Clock 10 = Receiver Clock 4 Times AD Clock 11 = Receiver Clock Equals AD Clock</p>
																<p>Software SYNC Bit (write only) Writing a 1h clears the packet counter used in the header.</p>
																<p>Packet Count Clear (write only) Writing a 1h clears the packet counter used in the header.</p>
																<p>Local Bus Reset Bit (write only) Writing a 1h resets local bus.</p>
																<p>Raceway Done A (read only) 0 = Raceway Busy 1 = Raceway DMA A Done</p>

Table 6-3 Command Status Register (continued)

Abbreviation	Width	Address Offset	Mask	Attribute												
CSR	32	0 0000h	001FFFFFF	R/W												
Least Significant Word																
1 5	1 4	1 3	1 2	1 1	1 0	9	8	7	6	5	4	3	2	1	0	Description
																Raceway Done B (read only) 0 = Raceway Busy 1 = Raceway DMA B Done Not Used
Most Significant Word																
3 1	3 0	2 9	2 8	2 7	2 6	2 5	2 4	2 3	2 2	2 1	2 0	1 9	1 8	1 7	1 6	Description
																Reserved (test bit) Receiver Clock Multiplier Channels 0-3 Enables 15mS for the PLL to stabilize as changing these bits. These are not available on the NR revision. 00 = Receiver Clock Equals AD Clock 01 = Receiver Clock 2 Times AD Clock 10 = Receiver Clock 4 Times AD Clock 11 = Receiver Clock Equals AD Clock Receiver Clock Multiplier Channels 4-7 Enables 15mS for the PLL to stabilize as changing these bits. These are not available on the NR revision. 00 = Receiver Clock Equals AD Clock 01 = Receiver Clock 2 Times AD Clock 10 = Receiver Clock 4 Times AD Clock 11 = Receiver Clock Equals AD Clock Not Used

Table 6-4 FIFO Flags Register

Abbreviation	Width	Address Offset	Mask	Attribute												
FLAGS	32	0 0004h	77777777	Read Only												
Least Significant Word																
1 5	1 4	1 3	1 2	1 1	1 0	9	8	7	6	5	4	3	2	1	0	Description
																<p>Channel 0 FIFO status 0000 = FIFO Empty 0001 = FIFO < 16 words 0011 = FIFO > or = 16 words 0111 = FIFO Full</p> <p>Channel 1 FIFO Current Status 0000 = FIFO Empty 0001 = FIFO < 16 words 0011 = FIFO > or = 16 words 0111 = FIFO Full</p> <p>Channel 2 FIFO Status Current Status 0000 = FIFO Empty 0001 = FIFO < 16 words 0011 = FIFO > or = 16 words 0111 = FIFO Full</p> <p>Channel 3 FIFO Current Status 0000 = FIFO Empty 0001 = FIFO < 16 words 0011 = FIFO > or = 16 words 0111 = FIFO Full</p>

Table 6-4 FIFO Flags Register (continued)

Abbreviation	Width	Address Offset	Mask	Attribute												
FLAGS	32	0 0004h	77777777	Read Only												
Most Significant Word																
3 1	3 0	2 9	2 8	2 7	2 6	2 5	2 4	2 3	2 2	2 1	2 0	1 9	1 8	1 7	1 6	Description
Channel 4 FIFO Current Status																
0000 = FIFO Empty																
0001 = FIFO < 16 words																
0011 = FIFO > or = 16 words																
0111 = FIFO Full																
Channel 5 FIFO Current Status																
0000 = FIFO Empty																
0001 = FIFO < 16 words																
0011 = FIFO > or = 16 words																
0111 = FIFO Full																
Channel 6 FIFO Current Status																
0000 = FIFO Empty																
0001 = FIFO < 16 words																
0011 = FIFO > or = 16 words																
0111 = FIFO Full																
Channel 7 FIFO Current Status																
0000 = FIFO Empty																
0001 = FIFO < 16 words																
0011 = FIFO > or = 16 words																
0111 = FIFO Full																

Table 6-5 Interrupt Vector Register

Abbreviation	Width	Address Offset	Mask	Attribute												
INTVEC	32	0 0008h	000000FF	Read/Write												
Least Significant Word																
1 5	1 4	1 3	1 2	1 1	1 0	9	8	7	6	5	4	3	2	1	0	Description
																8-bit Interrupt vector driven on the bus when the ECDR-814x interrupt is acknowledged by the VME interface.
																Not Used
Most Significant Word																
3 1	3 0	2 9	2 8	2 7	2 6	2 5	2 4	2 3	2 2	2 1	2 0	1 9	1 8	1 7	1 6	Description
																Not Used

Table 6-6 Interrupt Mask Register

Abbreviation	Width	Address Offset	Mask	Attribute												
INTMASK	32	0 000Ch	000007FF	Read/Write												
Least Significant Word																
1 5	1 4	1 3	1 2	1 1	1 0	9	8	7	6	5	4	3	2	1	0	Description
																<p>Channel 0 Data Available in the FIFO. Sets if the counted burst is complete or if the gate goes in active. 0h = Interrupt Disabled; 1h = Interrupt Enabled</p> <p>Channel 1 Data Available in the FIFO. Sets if the counted burst is complete or if the gate goes in active. 0h = Interrupt Disabled; 1h = Interrupt Enabled</p> <p>Channel 2 Data Available in the FIFO. Sets if the counted burst is complete or if the gate goes in active. 0h = Interrupt Disabled; 1h = Interrupt Enabled</p> <p>Channel 3 Data Available in the FIFO. Sets if the counted burst is complete or if the gate goes in active. 0h = Interrupt Disabled; 1h = Interrupt Enabled</p> <p>Channel 4 Data Available in the FIFO. Sets if the counted burst is complete or if the gate goes in active. 0h = Interrupt Disabled; 1h = Interrupt Enabled</p> <p>Channel 5 Data Available in the FIFO. Sets if the counted burst is complete or if the gate goes in active. 0h = Interrupt Disabled; 1h = Interrupt Enabled</p> <p>Channel 6 Data Available in the FIFO. Sets if the counted burst is complete or if the gate goes in active. 0h = Interrupt Disabled; 1h = Interrupt Enabled</p> <p>Channel 7 Data Available in the FIFO. Sets if the counted burst is complete or if the gate goes in active. 0h = Interrupt Disabled; 1h = Interrupt Enabled</p> <p>Raceway Timeout Interrupt 0h = Interrupt Disabled; 1h = Interrupt Enabled</p> <p>Raceway Done A Interrupt 0h = Interrupt Disabled; 1h = Interrupt Enabled</p> <p>Raceway Done B Interrupt 0h = Interrupt Disabled; 1h = Interrupt Enabled</p> <p>Not Used</p>

Table 6-6 Interrupt Mask Register (continued)

Abbreviation	Width	Address Offset	Mask	Attribute											
INTMASK	32	0 000Ch	000007FF	Read/Write											
Most Significant Word															
3	3	2	2	2	2	2	2	2	2	2	1	1	1	1	Description
1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	
Not Used															

Table 6-7 Interrupt Status Register

Abbreviation	Width	Address Offset	Mask	Attribute												
INTMASK	32	0 000Ch	000007FF	Read/Write												
Least Significant Word																
1 5	1 4	1 3	1 2	1 1	1 0	9	8	7	6	5	4	3	2	1	0	Description
																Channel 0 Data Available in the FIFO. Sets if the counted burst is complete or if the gate goes in active. 0h = No Interrupt; 1h = Interrupt Occurred
																Channel 1 Data Available in the FIFO. Sets if the counted burst is complete or if the gate goes in active. 0h = No Interrupt; 1h = Interrupt Occurred
																Channel 2 Data Available in the FIFO. Sets if the counted burst is complete or if the gate goes in active. 0h = No Interrupt; 1h = Interrupt Occurred
																Channel 3 Data Available in the FIFO. Sets if the counted burst is complete or if the gate goes in active. 0h = No Interrupt; 1h = Interrupt Occurred
																Channel 4 Data Available in the FIFO. Sets if the counted burst is complete or if the gate goes in active. 0h = No Interrupt; 1h = Interrupt Occurred
																Channel 5 Data Available in the FIFO. Sets if the counted burst is complete or if the gate goes in active. 0h = No Interrupt; 1h = Interrupt Occurred
																Channel 6 Data Available in the FIFO. Sets if the counted burst is complete or if the gate goes in active. 0h = No Interrupt; 1h = Interrupt Occurred
																Channel 7 Data Available in the FIFO. Sets if the counted burst is complete or if the gate goes in active. 0h = No Interrupt; 1h = Interrupt Occurred
																Raceway Timeout Interrupt 0h = No Interrupt; 1h = Interrupt Occurred
																Raceway Done A Interrupt 0h = No Interrupt; 1h = Interrupt Occurred
Raceway Done B Interrupt 0h = No Interrupt; 1h = Interrupt Occurred																
Not Used																
Most Significant Word																
3 1	3 0	2 9	2 8	2 7	2 6	2 5	2 4	2 3	2 2	2 1	2 0	1 9	1 8	1 7	1 6	Description
Not Used																

Table 6-8 Header Word 0 Status Register

Abbreviation	Width	Address Offset	Mask	Attribute												
HEAD0	32	0 0014h	FFFFFFFF	Read Only												
Least Significant Word																
1 5	1 4	1 3	1 2	1 1	1 0	9	8	7	6	5	4	3	2	1	0	Description
																<p>Packet Counter (Lower 16 Bits) These are the least significant bits to a 24-bit counter that counts the number of packets being collected at the A/D clock rate.</p>
Most Significant Word																
3 1	3 0	2 9	2 8	2 7	2 6	2 5	2 4	2 3	2 2	2 1	2 0	1 9	1 8	1 7	1 6	Description
																<p>Packet Counter (Upper 8 Bits) These are the most significant bits to a 24-bit counter that counts the number of packets being collected at the A/D clock rate.</p>
																<p>Channel 0 A/D Over Range Bit 0h = Not Over Range 1h = Over Range</p>
																<p>Channel 1 A/D Over Range Bit 0h = Not Over Range 1h = Over Range</p>
																<p>Channel 2 A/D Over Range Bit 0h = Not Over Range 1h = Over Range</p>
																<p>Channel 3 A/D Over Range Bit 0h = Not Over Range 1h = Over Range</p>
																<p>Channel 4 A/D Over Range Bit 0h = Not Over Range 1h = Over Range</p>
																<p>Channel 5 A/D Over Range Bit 0h = Not Over Range 1h = Over Range</p>
																<p>Channel 6 A/D Over Range Bit 0h = Not Over Range 1h = Over Range</p>
																<p>Channel 7 A/D Over Range Bit 0h = Not Over Range 1h = Over Range</p>

Table 6-9 Header Word 1 Status Register

Abbreviation	Width	Address Offset	Mask	Attribute												
HEAD1	32	0 0018h	FFFFFFFF	Read Only												
Least Significant Word																
1 5	1 4	1 3	1 2	1 1	1 0	9	8	7	6	5	4	3	2	1	0	Description
External Header Bits																
16 header bits received through the J4 connector from an external source.																
Most Significant Word																
3 1	3 0	2 9	2 8	2 7	2 6	2 5	2 4	2 3	2 2	2 1	2 0	1 9	1 8	1 7	1 6	Description
																Channel 0 FIFO Full Flag 0h = No Full Flag Detected, 1h = Full Flag
																Channel 1 FIFO Full Flag 0h = No Full Flag Detected, 1h = Full Flag
																Channel 2 FIFO Full Flag 0h = No Full Flag Detected, 1h = Full Flag
																Channel 3 FIFO Full Flag 0h = No Full Flag Detected, 1h = Full Flag
																Channel 4 FIFO Full Flag 0h = No Full Flag Detected, 1h = Full Flag
																Channel 5 FIFO Full Flag 0h = No Full Flag Detected, 1h = Full Flag
																Channel 6 FIFO Full Flag 0h = No Full Flag Detected, 1h = Full Flag
																Channel 7 FIFO Full Flag 0h = No Full Flag Detected, 1h = Full Flag
																Channel 0 FIFO Empty Flag 0h = No Empty Flag Detected, 1h = Empty Flag
																Channel 1 FIFO Empty Flag 0h = No Empty Flag Detected, 1h = Empty Flag
																Channel 2 FIFO Empty Flag 0h = No Empty Flag Detected, 1h = Empty Flag
																Channel 3 FIFO Empty Flag 0h = No Empty Flag Detected, 1h = Empty Flag
																Channel 4 FIFO Empty Flag 0h = No Empty Flag Detected, 1h = Empty Flag
																Channel 5 FIFO Empty Flag 0h = No Empty Flag Detected, 1h = Empty Flag

Table 6-9 Header Word 1 Status Register (continued)

Abbreviation	Width	Address Offset	Mask	Attribute												
HEAD1	32	0 0018h	FFFFFFFF	Read Only												
Most Significant Word																
3 1	3 0	2 9	2 8	2 7	2 6	2 5	2 4	2 3	2 2	2 1	2 0	1 9	1 8	1 7	1 6	Description
															Channel 6 FIFO Empty Flag 0h = No Empty Flag Detected, 1h = Empty Flag	
															Channel 7 FIFO Empty Flag 0h = No Empty Flag Detected, 1h = Empty Flag	

ECDR-814x Channel Register Space

Address Offset	Abbreviation	Register Name	Attribute
01 0000h	CSR_C01	Command/Status Register Channel 0 & 1	Read/Write
01 0004h	RDEC_C0	Receiver Decimation Register Channel 0*	Read/Write
01 0008h	RCTL_C0	Receiver Control Channel 0*	Read/Write
01 000Ch	DWS_C0	Data Window Size Channel 0*	Read/Write
01 0010h	RDEC_C1	Receiver Decimation Register Channel 1*	Read/Write
01 0014h	RCTL_C1	Receiver Control Channel 1*	Read/Write
01 0018h	DWS_C1	Data Window Size Channel 1	Read/Write
01 001Ch	GAIN_C01	Gain Channel 0 & 1**	Read/Write
01 0020h – 01 1FFC		Not Used	
01 2000h – 01 3FFCh	RREG_C0A	Receiver Register Space Channel 0A*	Read/Write
01 4000h – 01 5FFCh	RREG_C0B	Receiver Register Space Channel 0B*	Read/Write
01 6000h – 01 7FFCh	RREG_C1A	Receiver Register Space Channel 1A*	Read/Write
01 8000h – 01 9FFCh	RREG_C1B	Receiver Register Space Channel 1B*	Read/Write
01 A000h – 01 FFFCh		Not Used	Read/Write
02 0000h	CSR_C23	Command/Status Register Channel 2 & 3	Read/Write
02 0004h	RDEC_C2	Receiver Decimation Register Channel 2*	Read/Write
02 0008h	RCTL_C2	Receiver Control Channel 2*	Read/Write
02 000Ch	DWS_C2	Data Window Size Channel 2	Read/Write
02 0010h	RDEC_C3	Receiver Decimation Register Channel 3*	Read/Write
02 0014h	RCTL_C3	Receiver Control Channel 3*	Read/Write
02 0018h	DWS_C3	Data Window Size Channel 3	Read/Write
02 001Ch	GAIN_C23	Gain Channel 2&3**	Read/Write
02 0020h – 02 1FFC		Not Used	
02 2000h – 02 3FFCh	RREG_C2A	Receiver Register Space Channel 2A*	Read/Write
02 4000h – 02 5FFCh	RREG_C2B	Receiver Register Space Channel 2B*	Read/Write
02 6000h – 02 7FFCh	RREG_C3A	Receiver Register Space Channel 3A*	Read/Write
02 8000h – 02 9FFCh	RREG_C3B	Receiver Register Space Channel 3B*	Read/Write
02 A000h – 02 FFFCh		Not Used	Read/Write

*Not applicable when used as an AD board

** Available ECDR-814G/x only

ECDR-814x Channel Register Space (Continued)

Address Offset	Abbreviation	Register Name	Attribute
03 0000h	CSR_C45	Command/Status Register Channel 4 & 5	Read/Write
03 0004h	RDEC_C4	Receiver Decimation Register Channel 4*	Read/Write
03 0008h	RCTL_C4	Receiver Control Channel 4*	Read/Write
03 000Ch	DWS_C4	Data Window Size Channel 4	Read/Write
03 0010h	RDEC_C5	Receiver Decimation Register Channel 5	Read/Write
03 0014h	RCTL_C5	Receiver Control Channel 5	Read/Write
03 0018h	DWS_C5	Data Window Size Channel 5	Read/Write
03 001Ch	GAIN_C45	Gain Channel 4 & 5**	Read/Write
03 0020h – 03 1FFC		Not Used	
03 2000h – 03 3FFCh	RREG_C4A	Receiver Register Space Channel 4A*	Read/Write
03 4000h – 03 5FFCh	RREG_C4B	Receiver Register Space Channel 4B*	Read/Write
03 6000h – 03 7FFCh	RREG_C5A	Receiver Register Space Channel 5A*	Read/Write
03 8000h – 03 9FFCh	RREG_C5B	Receiver Register Space Channel 5B*	Read/Write
03 A000h – 03 FFFCh		Not Used	Read/Write
04 0000h	CSR_C67	Command/Status Register Channel 6 & 7	Read/Write
04 0004h	RDEC_C6	Receiver Decimation Register Channel 6*	Read/Write
04 0008h	RCTL_C6	Receiver Control Channel 6*	Read/Write
04 000Ch	DWS_C6	Data Window Size Channel 6	Read/Write
04 0010h	RDEC_C7	Receiver Decimation Register Channel 7*	Read/Write
04 0014h	RCTL_C7	Receiver Control Channel 7*	Read/Write
04 0018h	DWS_C7	Data Window Size Channel 7	Read/Write
04 001Ch	GAIN_C67	Gain Channel 6 & 7**	Read/Write
04 0020h – 04 1FFC		Not Used	
04 2000h – 04 3FFCh	RDATA_C6A	Receiver Register Space Channel 6A*	Read/Write
04 4000h – 04 5FFCh	RDATA_C6B	Receiver Register Space Channel 6B*	Read/Write
04 6000h – 04 7FFCh	RDATA_C7A	Receiver Register Space Channel 7A*	Read/Write
04 8000h – 04 9FFCh	RDATA_C7B	Receiver Register Space Channel 7B*	Read/Write
04 A000h – 04 FFFCh		Not Used	Read/Write

*Not applicable when used as an AD board

** Available ECDR-814G/x only

Table 6-10 Command/Status Register Channel 0 & 1 (2 & 3, 4 & 5, 6 & 7)

Abbreviation	Width	Address Offset	Mask	Attribute													
CSR_C01 (23, 35, 67)	16	01 0000h 02 0000h 03 0000h 04 0000h	1FFF	Read/Write													
Least Significant Word																	
1 5	1 4	1 3	1 2	1 1	1 0	9	8	7	6	5	4	3	2	1	0	Description	
																	<p>Acquisition Clock Configuration 0h = Receiver clock greater than the acquisition clock. 1h = Receiver clock the same as the acquisition clock.</p> <p>NCO Sync Enable Receiver Channels 0 & 1 (2&3, 4&5, 6&7). This bit is to enable Coherent Sampling - Starting the NCO at 0° Phase at the start of each Gate/Trigger. (CIC2, CIC5, and RCF Filters are always synchronized to the beginning of an acquisition). When in dual receiver mode the NCOs is synchronized regardless of this bit's setting: (0h = Disabled; 1h = Enabled).</p> <p>FIFO Flag Offset This register selects the FIFO Flag Offset such the transfer throughput is maximized. This is done by programming the Programmable Almost Empty Flag in the FIFOs, to the appropriate value, and the throttling the transfer when the FIFO data falls below this value. This value needs to be the same on all the channels and is representative of the Read Back Mode selected in the CSR register. This value is loaded into the FIFO when FIFO Flag write bit is written. 00: 1 Channel Mode (Offset = 16) 01: 2 Channel Mode (Offset = 8) 10: 4 Channel Mode (Offset = 4) 11: 8 Channel Mode (Offset = 2) Note: all channels should be set to the same value.</p> <p>FIFO Flag Write Writing a one to this bit programs the FIFO Flag Offset, as defined in this register, into the FIFO. This bit can be written at the same time as the FIFO Flag Offset bits.</p> <p>NCO 0 (2, 4, 6) Sync Writing a one to this bit issues a sync to the NCO in both receiver chips for channel 0. This sync is issued regardless of the NCO sync enable bit.</p>

Table 6-10 Command/Status Register Channel 0 & 1 (2 & 3, 4 & 5, 6 & 7) (continued)

Abbreviation	Width	Address Offset	Mask	Attribute												
CSR_C01 (23, 35, 67)	16	01 0000h 02 0000h 03 0000h 04 0000h	1FFF	Read/Write												
Least Significant Word																
1 5	1 4	1 3	1 2	1 1	1 0	9	8	7	6	5	4	3	2	1	0	Description
																<p>NCO 1 (3, 5, 7) Sync Writing a one to this bit issues a sync to the NCO in both receiver chips for channel 1. This sync is issued regardless of the NCO sync enable bit.</p>
																<p>Receiver 0A (2A, 4A, 6A) reset Writing a one to this bit resets this receiver.</p>
																<p>Receiver 0B (2B, 4B, 6B) reset Writing a one to this bit resets this receiver.</p>
																<p>Receiver 1A (3A, 5A, 7A) reset Writing a one to this bit resets this receiver.</p>
																<p>Receiver 1B (3B, 5B, 7B) reset Writing a one to this bit resets this receiver.</p>
																<p>FIFO Channel 0 (2, 4, 8) reset Writing a one to this bit resets this FIFO.</p>
																<p>FIFO Channel 1 (3, 5, 7) reset Writing a one to this bit resets this FIFO.</p>
																<p>Not Used</p>

Table 6-11 Receiver Decimation Register Channel 0 (2, 4, 6)*

Abbreviation	Width	Address Offset	Mask	Attribute												
RDEC_C0 (2, 4, 6)	16	01 0004h 02 0004h 03 0004h 04 0004h	3FFF	Read/Write												
Least Significant Word																
1 5	1 4	1 3	1 2	1 1	1 0	9	8	7	6	5	4	3	2	1	0	Description
																<p>Total Decimation for Receiver Channel 0 (2, 4, 6) The programmed value should equal one-half the Total Decimation of the AD6620 minus 1. This register must always be programmed to the correct value for the receiver channel to operate correctly when interleaving 2 receivers for an AD channel.</p> <p style="text-align: center;">Total Decimation Value = ----- - 1 2</p>
																Not Used

***Not applicable when used as an AD board**

Table 6-12 Receiver Control Channel 0 (2, 4, 6)

Abbreviation	Width	Address Offset	Mask	Attribute												
RCTL_C0 (2, 4, 6)	16	01 0008h 02 0008h 03 0008h 04 0008h	8FFF	Read/Write												
Least Significant Word																
1 5	1 4	1 3	1 2	1 1	1 0	9	8	7	6	5	4	3	2	1	0	Description
																<p>Mode Select</p> <p>000h Dual Receiver I and Q data / No accumulate 001h Single Receiver I and Q data / No accumulate 010h Dual Receiver I data to accumulator 011h Single Receiver I data to accumulator 100h Dual Receiver Q data to accumulator 101h Single Receiver Q data to accumulator 110h Raw data / No accumulate 111h Raw data to accumulator</p> <p>Selects number of accumulates</p> <p>0000 = accumulate by 1 0001 = accumulate by 2 0010 = accumulate by 4 0011 = accumulate by 8 0100 = accumulate by 16 0101 = accumulate by 32 0110 = accumulate by 64 0111 = accumulate by 128 1000-1111 = accumulate by 256</p> <p>Trigger Mode</p> <p>00: Channel Disabled. 01: Trigger Mode: The Sync input or software sync will start acquisition and continue acquisition. Acquisition is stopped by the burst counter if the FREE RUN bit is low, or by writing the TRIGGER CLEAR bit if the FREE RUN bit is high. 1x: Gate Mode: The Sync input starts acquisition and continue acquisition. Acquisition is stopped by the Sync Input going inactive. The software sync and the FREE_RUN bit should not be used in this mode.</p>

Table 6-12 Receiver Control Channel 0 (2, 4, 6) (continued)

Abbreviation	Width	Address Offset	Mask	Attribute													
RCTL_C0 (2, 4, 6)	16	01 0008h 02 0008h 03 0008h 04 0008h	8FFF	Read/Write													
Least Significant Word																	
1 5	1 4	1 3	1 2	1 1	1 0	9	8	7	6	5	4	3	2	1	0	Description	
																	<p>Free Run</p> <p>0: The Burst Counter controls the amount of data collected.</p> <p>1: Data is collected continuously upon receipt of a sync.</p>
																	<p>Count Enable</p> <p>0: AD Data</p> <p>1: Counting Test Pattern</p>
																	<p>Burst Count MSB for Receiver Channel 0 (2, 4, 6).</p> <p>This is the MSB for the Burst Count Value in the DWS_C0 register.</p>
																	<p>Not Used</p>
																<p>Trigger Clear (write only)</p> <p>Writing a 1 to this bit will stop the current acquisition cycle when the trigger mode is 01.</p>	

Table 6-13 Data Window Size Channel 0 (2, 4, 6)

Abbreviation	Width	Address Offset	Mask	Attribute												
DWS_C0 (2, 4, 6)	16	01 000Ch 02 000Ch 03 000Ch 04 000Ch	FFFF	Read/Write												
Least Significant Word																
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
																<p>Burst Count Value for Channel 0 (2, 4, 6). This is the acquisition sample count – the number of words that are acquired when a trigger is received. This value is used in conjunction with the Burst Count MSB defined in the RCTL_C0 register to create a 17-bit burst count.</p> <p>The value written should be 1 less than the desired total number of words to be collected.</p> <p>If the user is in the “Raw Data to Accumulator” mode with an accumulate of 1, then the value written should be 2 less than the desired total number of words to be collected. This is also true if the user is collecting only Single Receiver data and only decimating by 2.</p>

Table 6-14 Receiver Decimation Register Channel 1 (3, 5, 7)*

Abbreviation	Width	Address Offset	Mask	Attribute																																											
RDEC_C1 (3, 5, 7)	16	01 0010h 02 0010h 03 0010h 04 0010h	3FFF	Read/Write																																											
Least Significant Word																																															
<table border="1" style="display: inline-table; border-collapse: collapse;"> <tr> <td style="text-align: center;">1</td><td style="text-align: center;">1</td><td style="text-align: center;">1</td><td style="text-align: center;">1</td><td style="text-align: center;">1</td><td style="text-align: center;">1</td><td style="text-align: center;">0</td><td style="text-align: center;">9</td><td style="text-align: center;">8</td><td style="text-align: center;">7</td><td style="text-align: center;">6</td><td style="text-align: center;">5</td><td style="text-align: center;">4</td><td style="text-align: center;">3</td><td style="text-align: center;">2</td><td style="text-align: center;">1</td><td style="text-align: center;">0</td> </tr> <tr> <td style="text-align: center;">5</td><td style="text-align: center;">4</td><td style="text-align: center;">3</td><td style="text-align: center;">2</td><td style="text-align: center;">1</td><td style="text-align: center;">0</td><td style="text-align: center;">9</td><td style="text-align: center;">8</td><td style="text-align: center;">7</td><td style="text-align: center;">6</td><td style="text-align: center;">5</td><td style="text-align: center;">4</td><td style="text-align: center;">3</td><td style="text-align: center;">2</td><td style="text-align: center;">1</td><td style="text-align: center;">0</td> </tr> </table>											1	1	1	1	1	1	0	9	8	7	6	5	4	3	2	1	0	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	Description			
1	1	1	1	1	1	0	9	8	7	6	5	4	3	2	1	0																															
5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0																																
											<p>Total Decimation for Receiver Channel 1 (3, 5, 7) The programmed value should equal one-half the Total Decimation of the AD6620 minus 1. This register must always be programmed to the correct value for the receiver channel to operate correctly when interleaving 2 receivers for an AD channel.</p> <p style="text-align: center;">Total Decimation Value = $\frac{\text{-----}}{2} - 1$</p>																																				
											Not Used																																				

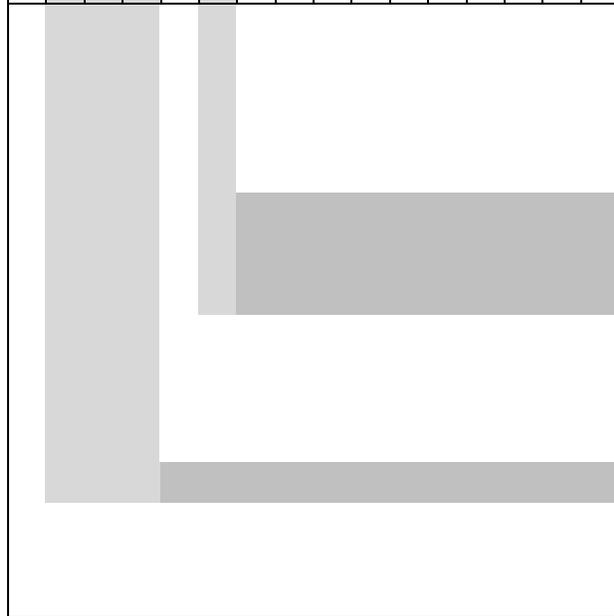
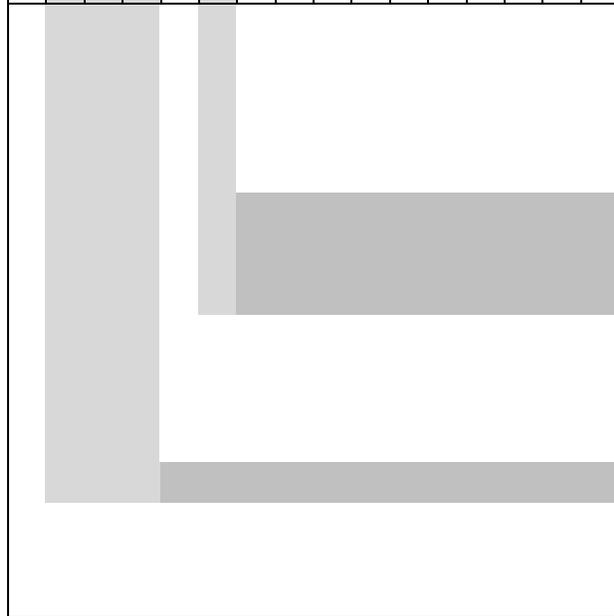
*** Not applicable when used as an A/D board**

Table 6-15 Receiver Control Channel 1 (3, 5, 7)*

Abbreviation	Width	Address Offset	Mask	Attribute												
RCTL_C1 (3, 5, 7)	16	01 0014h 02 0014h 03 0014h 04 0014h	8FFF	Read/Write												
Least Significant Word																
1 5	1 4	1 3	1 2	1 1	1 0	9	8	7	6	5	4	3	2	1	0	Description
																<p>Mode Select 000h Dual Receiver I and Q data / No accumulate 001h Single Receiver I and Q data / No accumulate 010h Dual Receiver I data to accumulator 011h Single Receiver I data to accumulator 100h Dual Receiver Q data to accumulator 101h Single Receiver Q data to accumulator 110h Raw data / No accumulate 111h Raw data to accumulator</p> <p>Selects number of accumulates 0000 = accumulate by 1 0001 = accumulate by 2 0010 = accumulate by 4 0011 = accumulate by 8 0100 = accumulate by 16 0101 = accumulate by 32 0110 = accumulate by 64 0111 = accumulate by 128 1000-1111 = accumulate by 256</p> <p>Trigger Mode 00: Channel Disabled 01: The Sync input or software sync will start acquisition and continue acquisition. Acquisition is stopped by the burst counter if the FREE RUN bit is low, or by writing the TRIGGER CLEAR bit if the FREE RUN bit is high. 1x: The Sync input will start acquisition and continue acquisition. Acquisition is by the Sync Input going inactive. The software sync and the FREE_RUN bit should not be used in this mode.</p> <p>Free Run 0: The Burst Counter controls the amount of data collected. 1: Data is collected continuously upon receipt of a sync.</p>

***Not applicable when used as an A/D board**

Table 6-15 Receiver Control Channel 1 (3, 5, 7)* (continued)

Abbreviation	Width	Address Offset	Mask	Attribute													
RCTL_C1 (3, 5, 7)	16	01 0014h 02 0014h 03 0014h 04 0014h	8FFF	Read/Write													
Least Significant Word																	
1	1	1	1	1	1	0	9	8	7	6	5	4	3	2	1	0	Description
																Free Run 0: The Burst Counter controls the amount of data collected. 1: Data is collected continuously upon receipt of a sync.	
																Count Enable 0: AD Data 1: Counting Test Pattern	
																Burst Count MSB for Receiver Channel 0 (2, 4, 6). This is the MSB for the Burst Count Value in the DWS_C0 register.	
																Not Used	
																Trigger Clear (write only) Writing a 1 to this bit will stop the current acquisition cycle when the trigger mode is 01.	

***Not applicable when used as an A/D board**

Table 6-16 Data Window Size Channel 1 (3, 5, 7)

Abbreviation	Width	Address Offset	Mask	Attribute												
DWS_C1 (3, 5, 7)	16	01 0018h 02 0018h 03 0018h 04 0018h	FFFF	Read/Write												
Least Significant Word																
1 5	1 4	1 3	1 2	1 1	1 0	9	8	7	6	5	4	3	2	1	0	Description
																<p>Burst Count Value for Channel 1 (3, 5, 7). This is the acquisition sample count – the number of words that will be acquired when a trigger is received. This value is used in conjunction with the Burst Count MSB defined in the RCTL_C1 register to create a 17-bit burst count.</p> <p>The value written should be 1 less than the desired total number of words to be collected.</p> <p>If the user is in the “Raw Data to Accumulator” mode with an accumulate of 1, then the value written should be 2 less than the desired total number of words to be collected. This is also true if the user is collecting only Single Receiver data and only decimating by 2.</p>

Table 6-17 Gain Channel 0 & 1 (2 & 3, 4 & 5, 6 & 7)*

Abbreviation	Width	Address Offset	Mask	Attribute												
GAIN_C01 (23, 35, 67)	16	01 001Ch 02 001Ch 03 001Ch 04 001Ch	0FFF	Read/Write												
Least Significant Word																
1 5	1 4	1 3	1 2	1 1	1 0	9	8	7	6	5	4	3	2	1	0	Description
																<p>Input Path Select Channel 0 (2, 4, 6) 0: No gain. Input signal is +5dBm full scale. 1: Gain is applied to the signal per register.</p> <p>Input Path Select Channel 1 (3, 5, 7) 0: No gain. Input signal is +5dBm full scale. 1: Gain is applied to the signal per register.</p> <p>Channel 0 (2, 4, 6) Gain This value is the gain applied to signal when the gain path is selected. The gain control has step size of 1dB with a full-scale input of -12 to 19dBm.</p> <p>00000b = -12dB 00001b = -11dB 00010b = -10dB 00100b = -8dB 01000b = -4dB 10000b = +4dB 11111b = 19dB</p> <p>Channel 1 (3, 5, 7) Gain: This value is the gain applied to signal when the gain path is selected. The gain control has step size of 1dB with a full-scale input of -12 to 19dBm.</p> <p>00000b = -12dB 00001b = -11dB 00010b = -10dB 00100b = -8dB 01000b = -4dB 10000b = +4dB 11111b = 19dB</p> <p>Not Used</p>

ECDR-814x Receiver Register Spaces

The ECDR-814x Receiver Register spaces are the same for each channel. Refer to the receiver memory map shown below.

Each receiver has two AD6620 receiver ICs (A or B), which must be programmed. Each space is broken into eight blocks, four for each receiver IC. When receiver #X is to be programmed, the X is replaced by 0A, 0B, 2A, 2B, ...7A, or 7B. Note that the Receiver Acquisition Clock must be connected before the receivers can be programmed.

Since the receiver registers require a 32-bit word, and the registers defined here are 16 bit, each register in the AD6620 requires two *reads* and two *writes* for each register in the AD6620. For example, to write to the register at 000h for receiver 1A, you write the lower 16-bits to 01 2000h and the upper 16 bits to 01 2004h. When the *write* to the upper 16 bits is executed, the onboard state machine takes both the lower and upper 16 bits and programs the registers in the AD6620.

Note: The following processing must occur for the AD6620 to be programmed correctly:

- The lower 16 bits must be written before the upper 16 bits.
- The lower 16-bits must be read from address 01 2000h followed by the upper 16-bits from 01 2004h.

Note: If the lower 16-bits are not read before the upper 16-bits then the data read does not represent what is in the AD6620.

Table 6-18 ECDR-814x Receiver Memory Map

Address Range Offset from Base Address	Description
0000h – 07FCh	Receiver #X RAM Coefficient Filter (RCF) Coefficient RAM
0800h – 0FFCh	Receiver #X RAM Coefficient Filter (RCF) Data RAM
1000h – 17FCh	Receiver #X Reserved
1800h – 1FFFh	Receiver #X Control Register Space

RCF Coefficient RAM

The RCF Coefficient RAM is the memory that stores user-programmable coefficients for the RCF filter. The RAM holds 256 20-bit two's complement words for a maximum filter length of 256 taps. In Dual Channel Real Mode, the filter length is limited to 128 taps per channel. N_{TAPS} controls the number of taps regardless of the number coefficient locations programmed.

RCF Data RAM

The RCF Data RAM stores I and Q data exiting the CIC5 filter stage while the RCF performs multiply accumulates. The lower 18 bits of Data RAM are I data; the upper 18 bits are Q data. The Data RAM is addressed in the memory map and can be accessed through the control ports so that the Data RAM can be flushed for testing and simulation purposes. The Data RAM is not cleared on reset, since this would have added additional hardware.

Note: Only the lower 32 bits are available. The four most significant bits have been omitted. Therefore, the lower 18 bits of the Data RAM (I data) can be completely read, but the upper four bits of the Q data are cut. Only the least significant 14 bits of the Q data can be seen.

ECDR-814x Receiver Control Register Space

The Receiver Control Register Space is the same for each of the eight receivers comprising the AD6620 Receiver IC.

Note: In the following table, under *Abbreviation* and *Register Name*, x represents the receiver number selected; y represents the receiver's AD6620, either A or B.

The tables following this section provide register information for the Receiver Control Register Space.

Table 6-19 Receiver Control Register Space

Address Offset	Abbreviation	Register Name	Attribute
1800 & 1804h	RxyMCR	Receiver #xy: Mode Control Register	Read/Write
1808 & 180Ch	RxyNCOC	Receiver #xy: NCO Control Register	Read/Write
1810 & 1814h	RxyNCOS	Receiver #xy: NCO Sync Control Register	Read/Write
1818 & 181Ch	RxyNCOF	Receiver #xy: NCO FREQ	Read/Write
1820 & 1824h	RxyNCOP	Receiver #xy: NCO Phase Offset	Read/Write
1828 & 1828h	RxyCIC2S	Receiver #xy: Input / CIC2 Scale Register	Read/Write
1830 & 1834h	RxyCIC2M	Receiver #xy: M _{CIC2} - 1	Read/Write
1838 & 183Ch	RxyCIC5S	Receiver #xy: S _{CIC5}	Read/Write
1840 & 1844h	RxyCIC5M	Receiver #xy: M _{CIC5} - 1	Read/Write
1848 & 184Ch	RxyRCFC	Receiver #xy: Output/RCF Control Register	Read/Write
1850 & 1854h	RxyRCFM	Receiver #xy: M _{RCF} - 1	Read/Write
1858 & 185Ch	RxyRCFA	Receiver #xy: RCF Address Offset Register	Read/Write
1860 & 1864h	RxyRCFN	Receiver #xy: N _{TAPS} - 1	Read/Write
1868 & 186Ch		Receiver #xy: Reserved (Should be written 00h)	Read/Write

This register brings the chip out of reset and sets the operating mode. The operating mode needs to be set to Sync Slave since the receivers on the ECDR-814 only function in this mode. It also specifies how the chip uses the SYNC pins: as outputs while acting as a sync master or as inputs while acting as a sync slave. This is the only register with a defined power-up state: on power up, each bit will be at a logic “1”. This places the chip in Soft Reset and defines the chip as a sync slave. Powering up to a sync slave avoids contention problems when connecting multiple AD6620s.

If bit 0 is written low and bits 2 & 1 are low, then the AD6620 is in Single Channel Real Mode. If bit 1 is high and bits 0 & 2 are low, then the device is in the Dual Channel Real Mode. If bit 2 is high and bit 0 & 1 are low, then the chip is in the Single Setting bit 3 high configures the AD6620 as a SYNC master; SYNC pins are then used as outputs. If bit 3 is low, then it is a SYNC slave, and the SYNC pins function as inputs. Bits 7-4 are reserved and should be written low.

Table 6-20 Mode Control Register

Abbreviation	Width	Address Offset	Mask	Attribute													
RxyMCR	16	1800	000F	Read/Write													
	16	1804h	0000														
Least Significant Word																	
1	1	1	1	1	1	9	8	7	6	5	4	3	2	1	0	Description	
5	4	3	2	1	0												Soft Reset
																	Dual Channel Real Input Mode
																	Single Channel Complex Input Mode
																	Sync Master/Slave (Master=1, Slave=0)
																	Reserved
																Not Used	
Most Significant Word																	
3	3	2	2	2	2	2	2	2	2	2	2	1	1	1	1	Description	
1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6		
																Not Used	

The NCO Sync Control Register holds the SYNC_MASK, which controls the frequency of the SYNC_NCO pulses and therefore the phase accuracy of the synchronization.

Table 6-22 NCO Sync Control Register

Abbreviation	Width	Address Offset	Mask	Attribute												
RxyNCOS	16 16	1810 1814h	FFFF FFFF	Read/Write												
Least Significant Word																
1 5	1 4	1 3	1 2	1 1	1 0	9	8	7	6	5	4	3	2	1	0	Description
Sync Mask LSW																
Most Significant Word																
3 1	3 0	2 9	2 8	2 7	2 6	2 5	2 4	2 3	2 2	2 1	2 0	1 9	1 8	1 7	1 6	Description
Sync Mask MSW																

This NCO FREQ register holds the NCO frequency control word. This is a 32-bit unsigned integer that sets the frequency of the AD6620 NCO.

Table 6-23 NCO FREQ

Abbreviation	Width	Address Offset	Mask	Attribute												
RxyNCOF	16 16	1818 181Ch	FFFF FFFF	Read/Write												
Least Significant Word																
1 5	1 4	1 3	1 2	1 1	1 0	9	8	7	6	5	4	3	2	1	0	Description
NCO Frequency LSW																
Most Significant Word																
3 1	3 0	2 9	2 8	2 7	2 6	2 5	2 4	2 3	2 2	2 1	2 0	1 9	1 8	1 7	1 6	Description
NCO Frequency MSW																

The NCO Phase Offset register controls the phase offset of NCO. This can be used to allow for phase differences between multiple antennas receiving the same carrier.

Table 6-24 NCO Phase Offset

Abbreviation	Width	Address Offset	Mask	Attribute											
RxyNCOP	16	1820	FFFF	Read/Write											
	16	1824h	FFFF												
Least Significant Word															
1 1 1 1 1 1 0 9 8 7 6 5 4 3 2 1 0															Description
															NCO Phase Offset LSW
Most Significant Word															
3 3 2 2 2 2 2 2 2 2 2 1 1 1 1 1 0 9 8 7 6															Description
															NCO Phase Offset MSW

The Input/CIC2 Scale register holds the scale factor, S_{CIC2} , for CIC2. S_{CIC2} scales down the data before it is accumulated in CIC2. This avoids register wrap-around in the twos-complement arithmetic and eliminates the resulting spectral errors. S_{CIC2} is contained in bits 2-0 of this register. It is treated as an unsigned integer between 0 and 6. Increasing S_{CIC2} shifts data down.

The second function of this register is to scale the input data from the Parallel Data Input port. This enables the AD6620 to treat the floating point input data with considerable flexibility. There are two parts of this function. The first is bit 4, which tells the AD6620 how to handle the exponent, EXP[2:0]. If this bit is low, then data is shifted down as the exponent increases. If this bit is high, then for increasing EXP[2:0] the input data is shifted up. The second part of the input data shifting is the Exponent Offset (ExpOff[7..5]) held in bits 7-5 of this register. This provides gain to the input.

Table 6-25 Input/CIC2 Scale Register

Abbreviation	Width	Address Offset	Mask	Attribute													
RxyCIC2S	16	1828	00FF	Read/Write													
	16	182Ch	0000														
Least Significant Word																	
1 5	1 4	1 3	1 2	1 1	1 0	9 8	7 6	5 5	4 4	3 3	2 2	1 1	0 0	Description			
													S_{CIC2}				
													Reserved				
													ExpInv				
													ExpOff				
													Not Used				
Most Significant Word																	
3 1	3 0	2 9	2 8	2 7	2 6	2 5	2 4	2 3	2 2	2 1	2 0	1 9	1 8	1 7	1 6	Description	
													Not Used				

The MCIC2 - 1 register controls the amount of decimation in the CIC2 filter stage. The value contained in this register is the CIC2 decimation rate minus one. This is interpreted as an unsigned 8-bit integer but due to limited growth in the CIC2 filter accumulators, this value should normally be limited to 15 (decimation =16).

Table 6-26 M_{CIC2} - 1

Abbreviation	Width	Address Offset	Mask	Attribute																	
RxyCIC2M	16 16	1830 1834h	00FF 0000	Read/Write																	
Least Significant Word																					
<table border="1" style="border-collapse: collapse; width: 100%;"> <tr> <td style="width: 20px; text-align: center;">1</td><td style="width: 20px; text-align: center;">0</td><td style="width: 20px; text-align: center;">9</td><td style="width: 20px; text-align: center;">8</td><td style="width: 20px; text-align: center;">7</td><td style="width: 20px; text-align: center;">6</td><td style="width: 20px; text-align: center;">5</td><td style="width: 20px; text-align: center;">4</td><td style="width: 20px; text-align: center;">3</td><td style="width: 20px; text-align: center;">2</td><td style="width: 20px; text-align: center;">1</td><td style="width: 20px; text-align: center;">0</td> </tr> </table>	1	1	1	1	1	1	0	9	8	7	6	5	4	3	2	1	0	Description			
1	1	1	1	1	1	0	9	8	7	6	5	4	3	2	1	0					
									CIC2 Decimation Minus One												
									Not Used												
Most Significant Word																					
<table border="1" style="border-collapse: collapse; width: 100%;"> <tr> <td style="width: 20px; text-align: center;">3</td><td style="width: 20px; text-align: center;">3</td><td style="width: 20px; text-align: center;">2</td><td style="width: 20px; text-align: center;">1</td><td style="width: 20px; text-align: center;">1</td><td style="width: 20px; text-align: center;">1</td><td style="width: 20px; text-align: center;">1</td> </tr> </table>	3	3	2	2	2	2	2	2	2	2	2	2	1	1	1	1	Description				
3	3	2	2	2	2	2	2	2	2	2	2	1	1	1	1						
Not Used																					

The MCIC - 1 register controls the amount of decimation in the CIC5 filter stage. The value contained in this register is the CIC5 decimation rate minus one. This is interpreted as an unsigned 8-bit integer but due to limited growth in the CIC5 filter accumulators, this value should normally be limited to 31 (decimation = 32).

Table 6-28 M_{CIC5} - 1

Abbreviation	Width	Address Offset	Mask	Attribute												
RxyCIC5M	16	1840	00FF	Read/Write												
	16	1844h	0000													
Least Significant Word																
1 5	1 4	1 3	1 2	1 1	1 0	9	8	7	6	5	4	3	2	1	0	Description
								CIC5 Decimation Minus One								
								Not Used								
Most Significant Word																
3 1	3 0	2 9	2 8	2 7	2 6	2 5	2 4	2 3	2 2	2 1	2 0	1 9	1 8	1 7	1 6	Description
																Not Used

Bits 2-0 of the Output/RCF Control register hold the Output Scale Factor, S_{OUT} . These bits are interpreted as a 3-bit unsigned integer; this value controls which of the 23 output bits of the RCF are passed to the output port being used. The data Output corresponds to the following equation where OL_{RCF} is the 23-bit output of the RCF and POL is the 16-bit data available at the parallel output port or the serial port when 16-bit serial words are used. The truncation function rounds the scaled 23-bit number to 16 bits. $POL = round(OL_{RCF} \times 2^{(S_{OUT}-1)}, 16)$

Note: Bits 7-3 of this register are reserved and must be written 0.

Table 6-29 Output/RCF Control Register

Abbreviation	Width	Address Offset	Mask	Attribute												
RxyRCFC	16	1848	00FF	Read/Write												
	16	184Ch	0000													
Least Significant Word																
1	1	1	1	1	1											Description
5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	
											Output Scale Factor					
											Reserved					
											Not Used					
Most Significant Word																
3	3	2	2	2	2	2	2	2	2	2	2	1	1	1	1	Description
1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	
											Not Used					

The MRCF - 1 register controls the amount of decimation in the RCF filter stage. The value contained in this register is the RCF decimation rate minus one. This is interpreted as an unsigned 8-bit integer, but due to limited number of taps and, therefore, filtering power in the RCF filter accumulators this value should be limited to 31 (decimation = 32).

Table 6-30 M_{RCF} - 1

Abbreviation	Width	Address Offset	Mask	Attribute												
RxyRCFM	16	1850	00FF	Read/Write												
	16	1854h	0000													
Least Significant Word																
1 5	1 4	1 3	1 2	1 1	1 0	9	8	7	6	5	4	3	2	1	0	Description
								RCF Decimation Minus One								
								Not Used								
Most Significant Word																
3 1	3 0	2 9	2 8	2 7	2 6	2 5	2 4	2 3	2 2	2 1	2 0	1 9	1 8	1 7	1 6	Description
Not Used																

The RCF Address Offset register controls the address offset used by the RCF to calculate a given filter and is interrupted as an 8-bit unsigned integer. It allows more than one filter to be placed in the Coefficient RAM. This makes it possible to switch filters without reloading all of the coefficients. The RCF filter computes taps for all coefficients between RCF_{OFF} and $(RCF_{OFF} + N_{TAPS})$ provided the decimation, clock rate, and input data rate provide sufficient time for this.

Table 6-31 RCF Address Offset Register

Abbreviation	Width	Address Offset	Mask	Attribute													
RxyRCFA	16	1858	00FF	Read/Write													
	16	185Ch	0000														
Least Significant Word																	
1 5	1 4	1 3	1 2	1 1	1 0	9	8	7	6	5	4	3	2	1	0	Description	
								Filter Coefficient Address Offset									
								Not Used									
Most Significant Word																	
3 1	3 0	2 9	2 8	2 7	2 6	2 5	2 4	2 3	2 2	2 1	2 0	1 9	1 8	1 7	1 6	Description	
																Not Used	

The $N_{TAPS} - 1$ register controls the number of taps calculated by the RCF. The value in this register is interpreted as an unsigned integer and is equal to the number of taps desired minus one. This filter is not inherently symmetric and the number of coefficients placed in the Coefficient RAM is equal to the number of taps, provided that only one filter at a time is loaded. No symmetry is assumed and pre-addition is not used. The total number of taps for all filters must be less than 256 taps for Single Channel Real Mode or less than 128 taps/channel for Diversity Channel Real Mode.

Table 6-32 $N_{TAPS} - 1$

Abbreviation	Width	Address Offset	Mask	Attribute												
RxyRCFN	16 16	1860 1864h	00FF 0000	Read/Write												
Least Significant Word																
1 5	1 4	1 3	1 2	1 1	1 0	9	8	7	6	5	4	3	2	1	0	Description
															Number of Taps Minus One	
															Not Used	
Most Significant Word																
3 1	3 0	2 9	2 8	2 7	2 6	2 5	2 4	2 3	2 2	2 1	2 0	1 9	1 8	1 7	1 6	Description
															Not Used	